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ABSTRACT

Traditional transistors based on complementary metal–oxide–semiconductor and metal–oxide–semiconductor field-effect transistors are facing significant limitations as device scaling reaches the limits of Moore's law. These limitations include increased leakage currents, pronounced short-channel effects, and quantum tunneling through the gate oxide, leading to higher power consumption and deviations from ideal behavior. Tunnel Field-Effect Transistors (TFETs) can overcome these challenges by utilizing the quantum tunneling of charge carriers to switch between on and off states and achieve a subthreshold swing below 60 mV/decade. This allows for lower power consumption, continued scaling, and improved performance in low-power applications. This review focuses on the design and operation of TFETs, emphasizing the optimization of device performance through material selection and advanced simulation techniques. The discussion will specifically address the use of two-dimensional materials in TFET design and explore simulation methods ranging from multi-scale approaches to machine learning-driven optimization.

I. INTRODUCTION

Despite the impressive performance of traditional complementary metal–oxide–semiconductor (CMOS) and metal–oxide–semiconductor field-effect transistors (MOSFETs) in the modern electronics industry, the acceleration of technological advancement is beginning to challenge the limits of Moore's law.[1–3] Consequently, alternative transistor devices[1,4–6] are being investigated with the objective of overcoming the performance issues that devices such as MOSFETs and CMOS are prone to present.[7] The optimal characteristics of a high-performing device include a small subthreshold swing (SS), low power consumption, minimal leakage current, and a high on/off current ratio.[8] In particular, an on/off current ratio of more than 10^4 is ideal, and being in the range of 10^3–10^4 is ideal for Tunnel Field-Effect Transistors (TFETs). An ideal range for the switching voltage is between 0.1 and 0.5 V. Nevertheless, the intrinsic switching mechanism of conventional semiconductor devices represents a significant limitation.[9,10] The operation of traditional semiconductor devices is based on p–n carrier transport, which restricts the SS of these devices to a value exceeding 60 mV/dec.[11] Moreover, this also constrains their capacity to achieve reduced power consumption.

By operating on a different switching mechanism, namely band-to-band tunneling (BTBT), TFETs can achieve a subthermal threshold swing of less than 60 mV/dec and gain access to a lower switching power.[12–16] Consequently, TFETs have been the subject of considerable research and development as a potential solution to the limitations of conventional FET-based devices. However, this same mechanism that enables these favorable characteristics also presents a trade-off between a low SS and a high on-current.[17]

The presence of indirect bandgaps and a low tunneling probability frequently results in the observation of relatively low on-current levels.[18] It is therefore crucial to consider the various aspects of TFET design, including material systems, supply and threshold voltages, device geometries, and other factors that can potentially impact the SS. The material system plays a pivotal role in optimizing the tunneling rate and reducing SS. In particular, heterojunctions[19] are of greater interest than homojunctions,[20] as single-material-based devices are unable to accommodate steep band profiles due to the presence of different doping levels.[11] The use of heterojunctions allows for the integration of disparate materials at the source and channel, thereby facilitating the formation of an abrupt interface.[21] This, in turn, permits a reduction in the width of the tunnel barrier and an increase in the tunneling probability.[22] The nature of TFET devices requires the band edges to be sharply defined at the interfaces. Accordingly, the design of the source–channel junction has a significant impact on the device's performance. The multi-scale (MS) modeling[23] of the TFET device is an indispensable component of the design optimization process. This requires the use of sophisticated software applications (e.g., Quantum ESPRESSO, Wannier90, and NanoTCAD ViDES).[24] The flexibility and adaptability of computational simulations are particularly advantageous in the identification and resolution of single-crystal defects and other design issues, as well as in the mitigation of other atomistic issues.

This review will address the salient features of TFET design and prediction, with a particular emphasis on two-dimensional (2D) heterojunction devices and the most prevalent materials utilized in their fabrication. The primary distinctions between the FET and TFET devices will be elucidated in Sec. II. Section III presents a comprehensive analysis of various 2D material systems and notable heterojunctions that have demonstrated significant potential for TFET device design. In Sec. IV, a variety of TFET material systems are examined, their simulated performances are detailed, and their potential for meeting the International Roadmap for Devices and Systems (IRDS) target requirements for high-performance future digital applications is discussed. The simulation of these devices is based on density functional theory (DFT) calculations, which predict the electronic structure and thermodynamic properties of channel materials. The calculation of a given material system's fundamental properties provides the basis for subsequent model development, enabling the prediction of device transfer characteristics. Section V examines the role of machine learning (ML)-based methods in facilitating the discovery of novel heterojunction materials.

II. KEY DIFFERENCES BETWEEN FETs AND TFETs

The fundamental distinction between MOSFETs and TFETs can be attributed to their disparate carrier transport and switching methodologies.[25] To fully comprehend this, it is essential to initially acknowledge that a MOSFET is a barrier-controlled device.[26] The application of a gate voltage is necessary to raise or lower the potential energy barrier between the source and the drain.[27] Once the energy barrier has been reduced to an adequate level, electrons from the source are able to traverse through the channel and reach the drain via thermionic emission [Fig. 1(a)].[28] This method of carrier transport presents significant challenges for the MOSFET downscaling process, which is otherwise known as short-channel effects (SCEs).[29] A reduction in the channel length of the device results in a decrease in effective doping, which, in turn, leads to a lowering

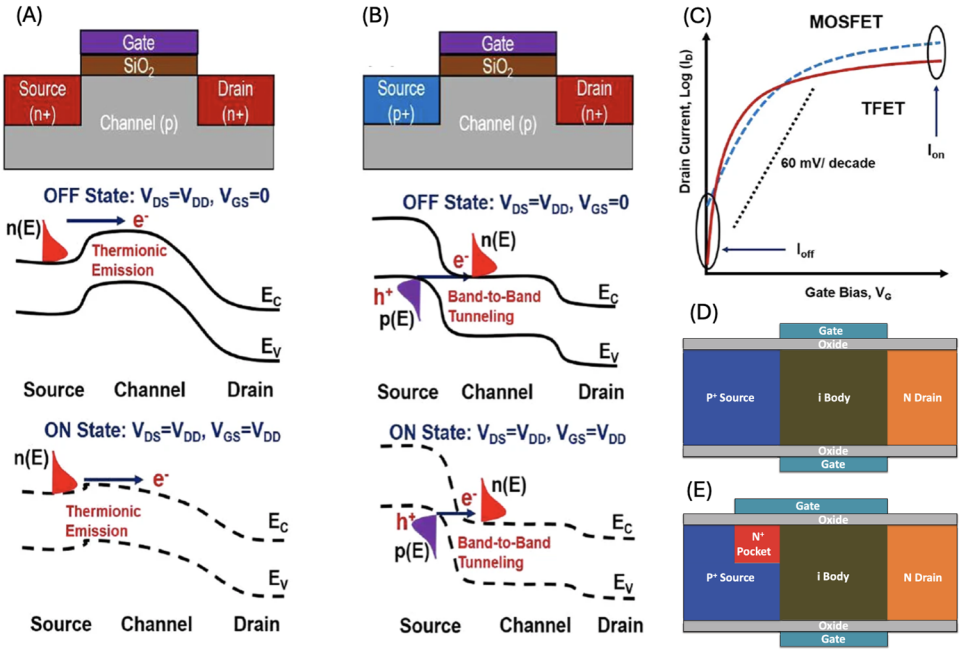


FIG. 1. Energy band diagram of (a) MOSFET, (b) TFET for on-state and off-state conditions, and (c) comparative transfer characteristics of well-designed MOSFET and TFET. Reproduced with permission from Kanungo *et al.*, npj 2D Mater. Appl. **6**(1), 83 (2022). Copyright 2022 Nature Publishing Group. Schematic of simulated devices: (d) lateral InAs TFET and (e) vertical InAs TFET with a heavily doped n+ pocket (halo) in the gate–source overlap region. Reproduced with permission from Ganapathi *et al.*, Appl. Phys. Lett. **97**, 033504 (2010). Copyright 2010 AIP Publishing LLC.[38]

of the threshold voltage (V_T). This correlation between the threshold voltage and the channel length provides insights into one of the primary SCEs,[27] namely, drain-induced barrier lowering (DIBL).[30] The application of a positive voltage to the drain results in a reduction in both the overall channel length and the threshold voltage of the device. This is due to the fact that the applied drain voltage results in an increase in the depletion layer, which, in turn, reduces the overall channel length and threshold voltage.[29] Furthermore, this SCE gives rise to a variation in the subthreshold current with high drain biases. A number of studies have examined potential solutions to this phenomenon and have identified several promising avenues for addressing it. These include reducing the thickness of the oxide,[29] increasing the doping concentration of the substrate, and exploring alternative doping methods,[31] such as halo[32–34] and pocket doping.[35–37]

The fundamental nature of MOSFETs is such that their carrier modulation is not only challenged by the SCEs that accompany it, but it is also inherently limited in its ability to achieve an SS below the thermal limit.[11] In particular, the Boltzmann distribution of charge carriers encounters a thermal limit of 60 mV/dec at room temperature. In contrast to MOSFET devices, where an applied gate voltage reduces the energy barrier and enables thermionic carrier emission, TFETs operate at a specific applied gate voltage where the bands at the source and channel are modulated to tune the width of the source–channel barrier [Fig. 1(b)]. When the width is sufficiently reduced, BTBT can occur, which results in a notable enhancement in the device's switching speed between its off and on states.[22,28] TFET devices employ this mechanism to facilitate electron tunneling through the energy barrier from the conduction band minimum (CBM) to the valence band maximum (VBM).[11] It is also noteworthy that an energy barrier exists in both the on and off states, which constrains the on-state performance. This allows for the achievement of a subthermal SS [Fig. 1(c)] and a significantly reduced power consumption in comparison with that of conventional FET devices.[28,39]

BTBT is a key physical mechanism underlying the operation of TFETs. It is a quantum mechanical phenomenon that allows charge carriers, such as electrons or holes, to directly "tunnel" through a potential energy barrier instead of going over it. This occurs because, according to quantum mechanics, particles exhibit a wave-like behavior, giving them a finite probability of penetrating through barriers that would not be possible in classical physics.

The likelihood of tunneling is strongly influenced by three primary parameters: the carrier effective mass, the bandgap energy, and the screening length. The effective mass determines how easily a carrier responds to external forces, while the bandgap represents the energy difference between the valence and conduction bands of a material. The screening length is a measure of how far electric fields penetrate into the material, affecting the width of the tunneling barrier. To maximize the tunneling probability, the objective is to minimize these three primary parameters, as smaller values of which result in a narrower and shorter barrier, thereby increasing the likelihood of tunneling.

A widely used model for calculating the tunneling probability is the Wentzel–Kramers–Brillouin (WKB) approximation. This semi-classical method estimates the transmission probability of a particle traversing a potential barrier. The WKB approximation expresses the tunneling probability as a function of the barrier's width and height, providing a foundational framework for understanding BTBT in TFETs. The following equation defines the transmission probability:

$$T_{\mathrm{WKB}} \approx \exp\left(\frac{-4\lambda E_g^{3/2}\sqrt{2m_t^*}}{3q\hbar(E_g+\Delta\phi)}\right),$$

where m_t is the effective mass of the tunneling carrier, E_g is the energy bandgap, $\hbar$ is the reduced Planck constant, q is the electronic charge, $\Delta\phi$ is the energy difference between the VBM and the CBM (energy window of tunneling), and λ is the screening length. The homogeneity of the material in homojunctions has been demonstrated to permit the WKB approximation to be precise in forecasting the existence of a solitary imaginary band that connects the real valence and conduction bands.[40] This subsequently represents the dominant tunneling pathway. However, this model is only applicable to devices based on a single material (homojunctions) as it tends to overestimate the tunneling current for devices based on more than a single material (heterojunctions).[28] At the interface of heterojunctions, a discontinuity is observed in the imaginary wave vectors obtained from the complex band structures of the constituent materials.[40] In light of these considerations, heterojunctions are more accurately predicted by models such as the Kane model or others.[41–43] It is of paramount importance to gain a precise understanding of the distinction between homojunctions and heterojunctions, as this affects the device's capacity to attain specific parameters. For example, when homojunctions exhibit disparate doping levels, it precludes the formation of a steep band profile, consequently broadening the width of the tunneling barrier.[44] In contrast, the nature of heterojunctions allows for a reduction in the tunneling distance and screening length, thereby enhancing the transmission probability. Moreover, heterojunction devices often display an elevated BTBT current due to the diminished distance between the conduction and valence bands in comparison with homojunction structures. In particular, a reduction in field strength is sufficient for the generation of high currents.

TFETs are designed to operate in accordance with an applied gate voltage, which modulates the width of the tunneling barrier. The gate voltage can only control the width of the tunneling junction barrier by increasing the channel inversion, which represents a form of indirect modulation of the tunneling barrier. The conventional TFET configuration comprises a single gate, isolated by a dielectric material, mounted over a channel situated between the source and drain electrodes.[31] Prior research has indicated that double-gated structures demonstrate a superior performance compared to single-gated TFETs. This is attributed to their capacity to mitigate ambipolar behavior and enhance the current within the device. A double-gated structure is precisely as its name suggests: an additional gate is placed parallel and opposite to the single gate, separated by dielectric layers. The use of heterojunctions of this kind can facilitate enhanced gate control due to the employment of a variety of gate materials with corresponding metal work functions. Furthermore, the double-gate structure has been shown to exhibit enhanced electrostatic control, a higher on/off current ratio, a higher on-current, and a lower off-current in TFET devices.[45]

In terms of their architectural specifications, TFET devices are further classified as either horizontal or vertical, which indicates the direction of tunneling within the device. In contrast to the lateral

carrier transport observed in horizontal TFET devices, BTBT in vertical TFETs can occur at an angle perpendicular to the gate oxide and channel interface.[46] The differentiation between these devices is based on the distinction between their respective mechanisms for transitioning between the off and on states. In a lateral device [Fig. 1(d)], when the gate voltage exceeds V_T, the tunneling barrier width becomes sufficiently thin for BTBT to occur, resulting in the overlap of the conduction and valence bands.[47] These conditions permit the occurrence of a substantial tunneling current, which, in turn, allows for a larger on-current. In the off state, the gate voltage is less than V_T, and BTBT is not permitted due to the tunneling barrier width exceeding the permitted thickness. In this state, although some leakage current does occur, it is not significant. In the off state of a vertical device, a thin barrier is maintained, yet the absence of band overlap precludes BTBT. This distinction enables the vertical TFET to achieve a more compact SS.[48] Vertical TFETs [Fig. 1(e)] permit direct modulation of the barrier width and enhanced gate control of BTBT. This shift in orientation has a significant impact on device performance, with vertical heterojunctions demonstrating superior capabilities compared to lateral heterojunctions. The regulation of the tunneling current through the gate voltage has enabled the achievement of a lower SS, which has resulted in a reduction in both the off current and power consumption.[48] The materials utilized for heterojunctions are distinct for the source and channel to achieve the requisite abrupt interface for the narrowing of the tunnel barrier width. Sections III A–III C will provide a more detailed examination of the various proposed structures.

III. 2D MATERIALS + HETEROJUNCTIONS SUITED FOR HIGH-PERFORMING TFET DEVICES AND OPTIMIZATION OF LOW SS

An ideal high-performing TFET device should exhibit the following key electrical characteristics: a small SS, low power consumption, high on-state current, and minimal leakage current.[49] The goal of TFET design is to achieve these essential electrical characteristics while minimizing the parameters that govern BTBT probability. Beyond SCEs that challenge MOSFETs, material selection emerges as a critical determinant of device performance. The bandgap of a material, an intrinsic property, plays a pivotal role in shaping the SS and tunneling behavior of a TFET. For instance, black phosphorus (BP) is particularly promising due to its adjustable bandgap, enabling precise optimization of the on/off current ratio for low-power applications. Group III–V materials, such as InAs and GaSb, are also notable for their narrow bandgap and high carrier mobility, which enhance tunneling efficiency and support higher on-state currents.[28] In addition, the exploration of new semiconductor materials is integral to mitigating SCEs.[50] Among these, 2D materials have attracted significant attention for TFET applications due to their high density of states (DOS), ultrathin body, and absence of dangling bonds, which collectively ensure superior electrostatic control.[51] However, challenges such as high leakage currents and low on-state currents persist, underscoring the importance of optimizing material properties to achieve the desired balance of TFET characteristics. They also highlight the trade-offs involved in optimizing one characteristic of TFET design at the expense of others, emphasizing the inherently multidimensional nature of this optimization problem. In this section, we examine the suitability of each material category—group III–V, transition metal dichalcogenides (TMDs), and BP—for TFET applications, comparing their strengths and limitations and analyzing the trade-offs between them.

A. Group III–V materials

Silicon (Si) is the material most commonly utilized in the contemporary semiconductor industry. The integration of TFET devices with Si allows for compatibility with existing fabrication processes and Si-based circuits, thereby facilitating the integration of new technology into existing infrastructure. Si, in particular, exhibits characteristics that are conducive to the development of TFETs. The indirect bandgap necessitates thermal activation for electron transitions, thereby facilitating the regulated reduction in off-state leakage. This is due to the fact that the thermal energy present at room temperature is insufficient to overcome the energy barrier. Germanium (Ge)-based TFETs have been the subject of investigation due to the favorable characteristics of germanium, including a small bandgap and high compatibility with Si.[52] In the context of transistors, where minimal heat dissipation is crucial for energy efficiency, indirect bandgap materials are typically preferred for fabrication due to their favorable characteristics, which include the ability to withstand high temperatures without significant degradation.

Nevertheless, indirect bandgap semiconductors exhibit suboptimal electron transitions due to a change in momentum, which can result in reduced energy dissipation, depending on the band structure.[52,53] In applications where the objective is to enhance energy efficiency by reducing thermal output, indirect bandgap semiconductors, such as Si, are frequently the preferred materials. In contrast, direct bandgap semiconductors demonstrate enhanced electronic transitions,[52] although this efficiency can result in elevated heat generation, which may be a disadvantage in certain applications. This renders them less suitable for applications involving traditional transistors. Nevertheless, they have been demonstrated to exhibit high efficiency with regard to BTBT in comparison with indirect bandgap materials. The direct bandgap enables direct electron tunneling with reduced energy requirements, resulting in a diminished SS, diminished off-state leakage current, and augmented energy efficiency.[54] Consequently, direct bandgap materials are preferred in the fabrication of TFETs due to the BTBT carrier injection method they employ.

Group III–V materials, including indium arsenide (InAs) and indium gallium arsenide (InGaAs), have emerged as pivotal compounds in the enhancement of TFET performance due to their distinctive semiconductor properties [Figs. 2(a)–2(d)].[19,55] InAs, with its low power bandgap of 0.35 eV, which is significantly lower than that of Si (1.12 eV), facilitates increased drain current through direct tunneling and is essential for achieving high on/off switching ratios in TFETs.[56] This quality renders it an especially attractive option for TFET applications, establishing it as a prevalent choice for group III–V TFET devices and a frequently featured material in relevant academic studies. The high electron mobility of InAs, which is several orders of magnitude greater than that of Si, is a significant contributing factor to this enhanced performance. However, this low bandgap also introduces certain trade-offs. While the reduced bandgap enhances tunneling probability, leading to higher on-state currents and improved on/off ratios, it also increases the likelihood of thermal leakage currents, which can compromise the off-state

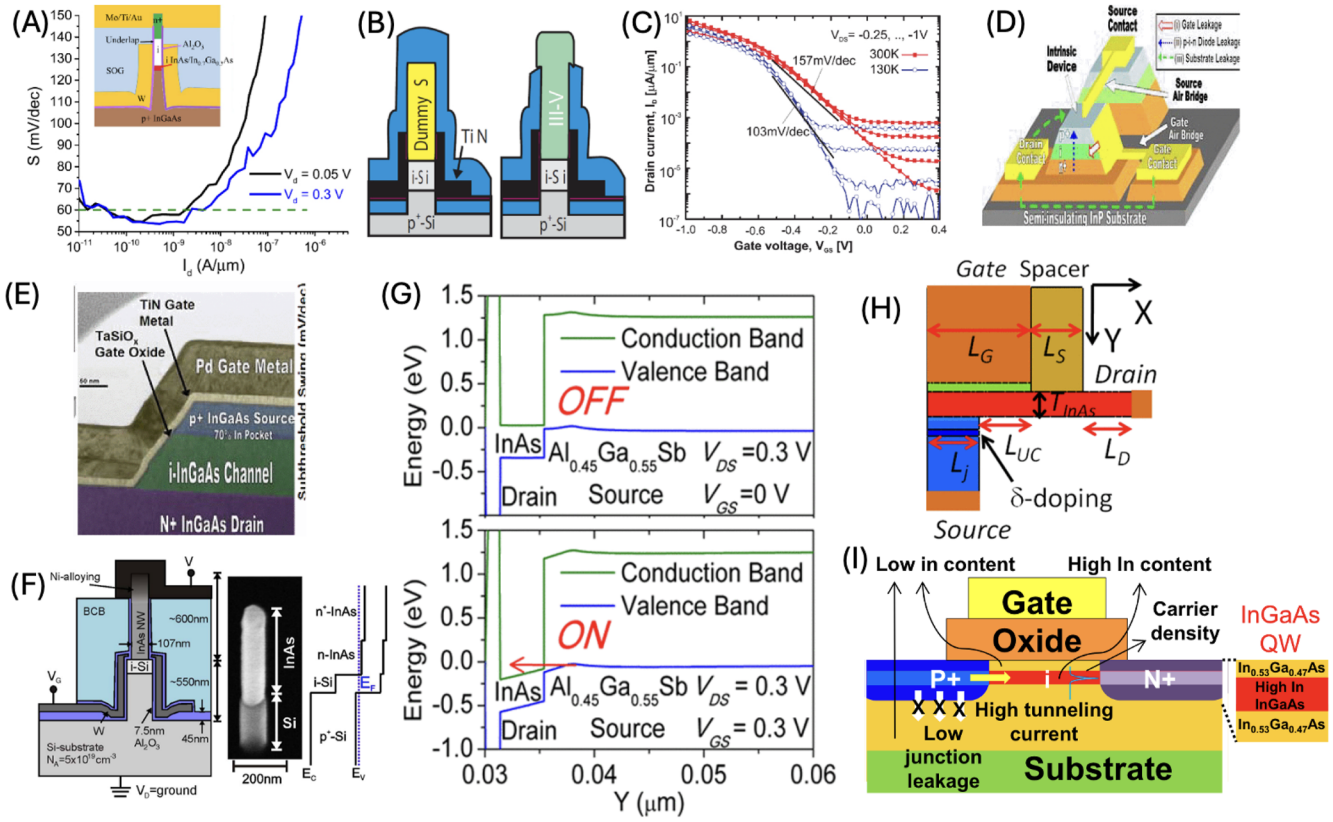


FIG. 2. (a) SS vs I_{DS} for a TFET fabricated using an etched InGaAs/InAs heterostructure, demonstrating subthermal transport over two decades of current. (b) Example of template-assisted selective epitaxy (TASE) of a TFET heterostructure in a vertical nanowire. (c) Transfer characteristics of such a device. Reproduced with permission from Convertino *et al.*, J. Phys.: Condens. Matter **30**, 264005 (2018). Copyright 2018 IOP Publishing. (d) Schematic of the InGaAs heterojunction TFET with a 5 μm thick body and single gate. From Dewey *et al.*, *2012 Symposium on VLSI Technology (VLSIT)*. Copyright 2012 IEEE. Reproduced with permission from IEEE. (e) TEM micrograph of the InGaAs heterojunction TFET showing the 4 nm ALD TaSiOx gate dielectric and the TiN/Pd metal gate. From Dewey *et al.*, *2012 Symposium on VLSI Technology (VLSIT)*. Copyright 2012 IEEE. Reproduced with permission from IEEE. (f) Schematic of the InAs nanowire (NW) TFET and the SEM image showing a heterojunction NW after DRIE of Si. Ozone cleaning followed by HF treatments causes shrinking of the InAs compared with Si. To the right is a schematic of the energy band edge diagram. Reproduced with permission from Moselund *et al.*, IEEE Electron Device Lett. **33**, 1453–1455 (2012). Copyright 2012 IEEE. (g) On top, energy-band diagrams in the off state: V_{DS} = 0.3 V and V_{GS} = 0 V. On bottom, energy-band diagrams in the on state: V_{DS} = V_{GS} = 0.3 V. Reproduced with permission from Lu *et al.*, IEEE Electron Device Lett. **33**, 655–657 (2012). Copyright 2012 IEEE. (h) Two-dimensional cross section of the simulated AlGaSb/InAs staggered-gap n-channel TFET device structure. Reproduced with permission from Lu *et al.*, IEEE Electron Device Lett. **33**, 655–657 (2012). Copyright 2012 IEEE. (i) Proposed InGaAs quantum well (QW) structure. Reproduced with permission from Takagi *et al.*, *2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems and Steep Transistors Workshop (E3S)*. Copyright 2017 IEEE. Reproduced with permission from IEEE.

performance and energy efficiency. Achieving a steep SS in InAs-based TFETs can be challenging due to difficulties in suppressing thermal generation currents at low gate voltages. These trade-offs underscore the need for careful optimization in device design, such as employing heterostructures or dual-gate architectures to balance high on-current, low SS, and minimal leakage current.[55,56]

Recent research has further demonstrated the potential of InAs-based devices when incorporated into heterostructures, such as InGaAs/GaAsSb and InAs/GaSb [Figs. 2(e)–2(i)], with promising results.[38,52,56,57,59] These studies, including one by Dutta *et al.*, have exploited the properties of InAs to achieve SS as low as 61.2 mV/dec and on/off ratios up to 7.13×10^4 in InAs-based double gate TFETs (see Table I for performance parameters). Recent advances in device engineering, such as the use of strained InAs[59] or integration with GaSb source materials, have shown promise in addressing performance trade-offs, enabling substantial improvements in both on-state and off-state performance. These findings firmly establish InAs as a strong candidate for low-power, high-performance TFET applications.

The research conducted by Takagi *et al.*[57] explored an InGaAs/GaAsSb heterostructure [Fig. 2(f)], achieving an even higher on/off ratio of 10^9 and a saturation speed of ~30 mV/dec.[57] The selection of materials was deliberate, with the objective of targeting small and direct bandgaps to enhance TFET on currents. Furthermore, they proposed a quantum well device with a Zn-diffused source region, which not only enhances the on current but also mitigates the off current due to the thin quantum well design, thereby attaining high on/off ratios at room temperature.

TABLE I. Summary of key performance metrics of various TFET designs, including their on-current, SS, and threshold voltage. Reproduced with permission from Dutta *et al.*, Int. J. Mod. Educ. Comput. Sci. **10**, 65–73 (2018). Copyright 2018 MECS Publisher.

	Device performance parameters			
Tunnel FET device	Subthreshold swing (SS) in mV/dec	On current (I_{on}) in mA/um	Off current (I_{off}) in nA/um	I_{on} to I_{off} ratio
Double gate Si TFET	116.3	0.002 52	9.43×10^{8}	10^{11}
Heterojunction double gate TFET	95.64	0.020 1	0.196	1.53×10^{4}
InAs based double gate TFET	61.2	0.24	3.39	7.13×10^{4}

The comprehensive review by Kumar Kumawat *et al.*[31] corroborates these findings, thereby reinforcing the notion that III–V compound semiconductors are the optimal choice for the source and drain in heterojunction TFETs.[31] The employment of materials with diminished direct bandgaps has been evidenced to augment device functionality, elevating the on-current and mitigating the off-current. This, in turn, results in enhanced outcomes for leakage current and SS. Convertino *et al.*[55] have demonstrated the versatility of III–V heterostructures through their exploration of InAs/GaSb, InAs/Si, and InGaAs/GaAsSb TFET structures.[55] The findings indicate that while InAs/GaSb nTFETs encounter performance issues related to depletion and gate stack optimization, InAs/Si pTFETs demonstrate promising outcomes with an average SS of ~70 mV/dec. Moreover, the InGaAs/GaAsSb system has been put forth as a means of accommodating both p- and n-channel devices, thereby offering a potential avenue for the development of complementary TFET technologies.

The encouraging outcomes of III–V heterostructures in TFET applications (Table I) underscore the significance of continued research and development in this field. By continuing to leverage the properties of these materials, such as high electron mobility and direct tunneling facilitated by narrow bandgaps, the enhancements of TFET performance can facilitate the development of low-power and higher-efficiency electronic devices.

B. Transition metal dichalcogenides (TMDs)

2D TMDs are distinguished by their ultra-thin body, which enhances gate control and reduces SCEs.[60] Due to their stackable nature and tunable thickness, TMDs can be precisely configured to exhibit a desired band structure and electronic properties, including the bandgap.[61] Multilayer TMDs typically exhibit indirect bandgaps, making monolayer TMDs—possessing direct bandgaps—more conducive to TFET experimentation. TMD materials, such as molybdenum disulfide (MoS_2) and tungsten disulfide (WS_2), possess direct bandgaps, which are optimal for the tunneling carrier injection mechanism within a TFET device. In addition, TMDs offer a high on/off current ratio, low SS, and high carrier mobility, making them promising candidates for TFET applications.

However, these advantages come with trade-offs. The relatively large bandgaps of TMDs, which typically exceed 1 eV, limit their ability to achieve the high drive current required for logic applications in TFETs, particularly at low operating voltages.[62] While smaller bandgaps, such as those exhibited by group III–V materials, are advantageous for high-speed switching and low-power operation, they are also associated with higher thermal leakage currents and reduced energy efficiency. In contrast, the larger bandgaps of TMDs provide superior thermal and electrical stability, which is crucial for hybrid TFET designs, high-reliability applications, and scenarios requiring extended operational lifetimes. These trade-offs necessitate a careful consideration of the target application when selecting TMDs as a channel material. For instance, in designs prioritizing low SS and high on/off ratios over maximum drive current, TMDs remain a highly advantageous option. Moreover, TMDs' compatibility with heterostructure integration and their ability to form van der Waals contacts with other materials offer further opportunities for optimizing device performance across diverse applications.[63]

In a study conducted by Joshi *et al.*, the $MoTe_2$ TFET was proposed as a device for visible light detection and photosensor applications.[64] The device configuration employed was a Dual-Material Gate (DMG)-TFET, wherein $MoTe_2$ was utilized as the channel material, exhibiting a thickness of 0.65 nm and a channel length of 100 nm.[64] The employment of this TMD material was found to result in a low energy bandgap (0.8–0.11 eV), which yielded high on-current and high sensitivity for the photosensor (high transmission in the visible range) in comparison with other TMDs. Furthermore, WTe_2 has been identified as a promising candidate for TFET due to its superior on-current characteristics and reduced DIBL effects [Fig. 3(a)]. This is due to the fact that, in comparison with $MoTe_2$, WTe_2 exhibits smaller in-plane dielectric constants, which reduce electric field penetration from the drain and suppress SCEs. Notwithstanding the larger bandgap of WTe_2, the on-current is situated in closer proximity to the threshold voltage. This phenomenon can be attributed to the lower dielectric constants of WTe_2, which enhance the on-current. For this TFET, the minimum achievable current is exceedingly low, remaining below 1 nA/μm even with higher drain doping levels [Figs. 3(b) and 3(c)]. In light of these observations, it can be concluded that WTe_2 is a promising candidate for TFET applications, as evidenced by its superior performance in various metrics, including on-current, SS, DIBL, and energy-delay product (EDP). These findings underscore the importance of considering not only thin-channel materials but also the optimal combination of bandgap, effective mass, and doping concentrations to achieve high-performance TFETs. It is evident that the mere thinning of materials is insufficient for optimizing device performance; attention must also be paid to the design choices surrounding the epitaxial layer thickness, body thickness, and doping levels.

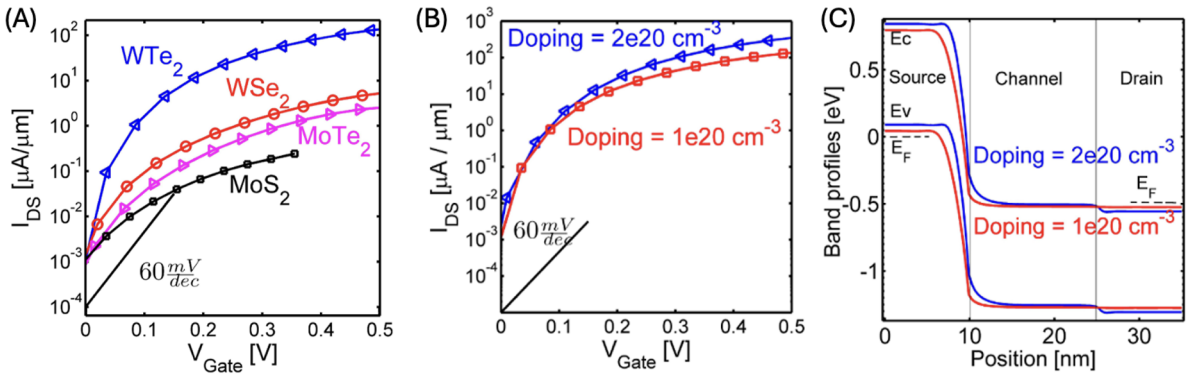


FIG. 3. High performance of TMD materials. (a) Transfer characteristics of TMD TFETs with I_{OFF} = 1 nA/μm. (b) Transfer characteristics and (c) band diagrams of WTe_2 with doping levels of 1×10^{20} and 2×10^{20} cm^{-3}. Reproduced with permission from Ilatikhameneh *et al.*, IEEE J. Explor. Solid-State Comput. Devices Circuits **1**, 12–18 (2015). Copyright 2015 IEEE.

C. Black phosphorous (BP)

BP has emerged as a leading contender for next-generation TFETs,[65] largely due to its distinctive properties as a 2D material. Its high electron mobility is instrumental in facilitating rapid charge transport, which is crucial for high-speed electronic devices.[66] It is noteworthy that the electron mobility in monolayer BP is high, reaching ~10 000 cm^2/V s. In contrast, the electron mobility is observed to decrease to ~1000 cm^2/V s in multilayered structures. This variation in mobility with thickness allows for precise engineering of a transistor's electrical properties, enabling optimization for specific applications.[67] Furthermore, BP's direct bandgap, which is layer-dependent, offers the ability to precisely tune the transistor's operating wavelength, making it highly suitable for optoelectronic and low-power digital applications. The electrical conductivity of BP can be effectively modulated by controlling the thickness, achieving on/off ratios of up to 10^4–10^5, which is advantageous for digital switches where distinct states of current flow are essential.[68]

While its tunable bandgap and thickness-dependent properties provide significant flexibility, they also introduce challenges related to material stability and device reliability. BP is highly susceptible to oxidation and degradation when exposed to ambient conditions, which can compromise its electronic properties and long-term performance. This necessitates encapsulation or protective coatings, which can increase fabrication complexity and impact device scalability.[65] In addition, although its tunable bandgap enhances on/off ratios and enables operation at low power, the relatively large bandgap in monolayer BP can limit the achievable drive current for certain high-performance logic applications. Meanwhile, the smaller bandgap in multilayer BP, while improving tunneling currents, may lead to higher leakage currents and reduced energy efficiency, particularly under off-state conditions. These trade-offs underscore the importance of balancing device design considerations, such as layer thickness, bandgap tuning, and environmental stability, to fully harness BP's potential for TFET applications.

An array of BP-based devices has demonstrated the potential for applications that require low-power and efficient switching, as evidenced by experimental results.[69] Among these, a BP TFET with modulated thickness is worthy of particular note for its suitability for low-power applications.[70] Kim *et al.* have developed two BP natural heterojunction (NHJ)-TFETs at $V_D \leq 0.7$ V: device 1 has a bottom-gate dielectric of 285-nm SiO_2 and a top-gate dielectric of 10-nm hBN, and device 2 has a bottom-gate dielectric of 3-nm hBN and a top-gate dielectric of 5-nm hBN. The BP device 1 exhibits a low SS of 23.7 mV/dec [Fig. 4(a)], with an averaged value of 4–5 decades. Furthermore, the device exhibits a considerable on-current, the measured drain current (I_D) vs V_{TG} showing I_{60} = 0.65 μA/μm. A noteworthy advancement has been the demonstration of BP TFETs with bilayer hBN tunnel barriers at the drain contact as highly promising switching devices. The bilayer hBN construction resulted in superior device efficiency, as indicated by an I_{60} of 0.65 μA/μm and an SS of <60 mV/dec (averaged for four decades) at 300 K.[71] The bilayer hBN exhibited a markedly reduced V_T change of 0.1 V, in stark contrast to the typical 0.7 V change observed in conventional MOSFETs. Moreover, the pivotal function of hBN was investigated in a BP device that demonstrated a remarkable performance, with a record-high I_{60} of 19.5 μA/μm at a drain voltage (V_D) of −0.7 V (p-type) and an SS = 37.6 mV/dec (averaged for four decades) at 300 K. In contrast, Wu *et al.* presented an alternative complementary BP TFET design that exhibited disparate characteristics, as shown in Fig. 4(b).[72] The findings indicated that the minimum SS was 178 mV/dec, which exceeded the Boltzmann limit significantly. This was attributed to the thickness of the BP flake used, which ranged from 8 to 13 nm. By precisely adjusting the channel thickness and reducing the equivalent oxide thickness (ETO) to ~0.5 nm, the researchers were able to significantly enhance the performance, resulting in an on-current of 800 μA/μm and an SS of 12 mV/dec.

The integrity of a semiconductor's crystal lattice is of paramount importance with regard to the electronic properties exhibited by the material. Similarly, the electronic characteristics of BP are closely related to its structural purity,[66] thereby reinforcing the importance of high-quality material synthesis for advanced electronic applications such as TFETs. Consequently, the achievement of single-crystalline 2D materials represents a crucial objective within the domain of semiconductor device fabrication. By

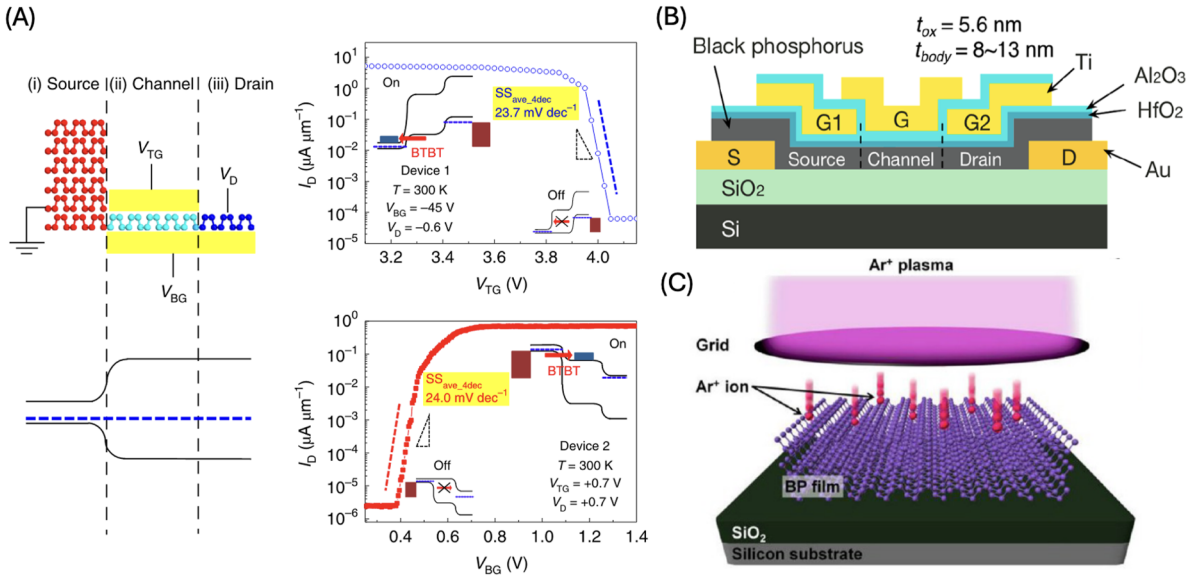


FIG. 4. (a) BP natural heterojunction (NHJ)-TFET schematic structure and BP band diagram in the (i) source, (ii) channel, and (iii) drain. Reproduced with permission from Kim *et al.*, Nat. Nanotechnol. **15**, 203–206 (2020). Copyright 2020 Nature Publishing Group. (b) Schematic of the BP reconfigurable electrostatically doped (RED) TFET. Reproduced with permission from Wu *et al.*, ACS Nano **13**, 377–385 (2019). Copyright 2019 American Chemical Society. (c) Schematic representation of the Ar+ plasma treatment process to BP for defect-tailoring. Reproduced with permission from Kang *et al.*, ACS Photonics **4**, 1822–1830 (2017). Copyright 2017 American Chemical Society.

modulating the thickness of the material, it is possible to tailor BP in order to reduce the incidence of interface defects.[66,67,70] Defects of this nature, including those of a lattice mismatch at surfaces, not only impair the intrinsic properties of the material in question but can also introduce trap levels that impede the flow of charge. In an ideal semiconductor, the absence of impurities and defects would result in the absence of electronic states within the bandgap. However, the presence of impurities, such as transition metals, often results in the formation of deep levels, which are energy states situated at a considerable distance from the bandgap edges. Such defects can function as traps for charge carriers, thereby impeding the conductivity of the device.[66]

Defects in BP can be classified according to three criteria: the nature of the bond, the structural distortions they induce, and the manner in which the bonds are broken. Such structural deformations, including vacancies in the crystal lattice, have the potential to significantly alter the bandgap energy of the material. For instance, a modified BP with a divacancy of the P1–P2 type (where P1 and P2 indicate the positions of two phosphorus atoms) has the potential to undergo a transition from its characteristic direct bandgap to an indirect one, with a value of 1.02 eV.[66] This transition is particularly disadvantageous for TFET designs, as these devices are optimized for BTBT, which is more effective with direct-bandgap semiconductors. The probability of tunneling is higher with direct BTBT due to the alignment of the valence and conduction bands in k-space, which facilitates a direct recombination of electrons and holes.[28] To optimize BP for TFETs, it is essential to implement high-purity fabrication and effective defect management. Techniques such as optimized chemical vapor deposition[74] or annealing[75] can be employed to mitigate defect-induced alterations to the bandgap.

It is noteworthy that controlled defect engineering[67] could potentially be employed to precisely adjust BP's electronic properties for specific device functions or to develop novel semiconductor devices that operate on disparate principles, such as resonant tunneling. An example from Kang *et al.* is using an argon plasma treatment process to BP for defect-tailoring, as shown in Fig. 4(c).[73] Despite the inherent challenges, defects can be harnessed to enhance TFET functionality when managed strategically.

IV. MULTI-SCALE SIMULATIONS

MS simulations are an indispensable tool for advancing TFETs, as they provide insights that are not readily accessible through experimental techniques alone.[24] They facilitate a comprehensive assessment of material properties, device physics, and operational characteristics at the nanoscale,[76] which are crucial for optimizing the performance and reliability of these devices. By employing MS simulations, a wide range of materials (including homojunction[24] and heterojunction materials[77] and device geometries) can be explored to identify optimal TFET designs, thus obviating the monetary costs and time consumption associated with the experimental testing of physical prototypes.[78] As device dimensions continue to decrease, traditional fabrication techniques and materials may introduce additional opportunities for error, necessitating the development of new approaches to ensure the reliability of the final product. MS simulations can thus anticipate these issues and allow for adjustments in either the design or the materials used to avoid them.[79] Similarly, the electrical characteristics of TFETs can be simulated under a variety of conditions to provide key performance

metrics, including on/off ratios, SS, and overall efficiency. A comparison of these characteristics with the requirements set out in the International Technology Roadmap for Semiconductors (ITRS) and with those of other devices is essential for the advancement of TFET technology.

The domain of MS simulations is anchored in three main categories: heterojunctions, homojunctions, and the emergent class of 2D materials. In this discussion, we will examine the complexities of simulation effectiveness across these domains, with a particular focus on the intricacies of TMD heterojunction simulations, the dynamics of BP homojunctions, and 2D materials such as arsenene (As), antimonene (Sb), and monolayer BP. In this section, we present a synthesis of findings from the existing literature to provide a comprehensive overview. In addition, we evaluate the range of their applications in different sectors and assess their significance in relation to the goal of advancing functionality and innovation within TFET technologies. The efficacy of MS simulations in this context for MOSFET development and material exploration underscores the pivotal role of MS simulations in propelling the advancement of TFET technology.

A. Framework of quantum simulations

The application of an *ab initio* quantum framework that integrates DFT, maximally localized Wannier functions (MLWFs), and non-equilibrium Green functions (NEGFs) facilitates the accurate estimation of transport properties and comprehensive device performance. This is a critical element in the process of guiding experimental design and device optimization. The steps required to perform these simulations and predict the transport properties of transistor devices and their framework are outlined in Fig. 5(a).[24,80] In the first step, a DFT package (e.g., Quantum ESPRESSO) is used to perform a series of calculations that predict not only the electronic structure but also the thermodynamic properties, providing a comprehensive picture of the intrinsic properties of the channel material. The Hamiltonian of the channel material is then transformed from a Bloch basis of extended eigenstates to a basis of MLWFs by Wannier90. These Wannier functions defined in terms of Bloch eigenstates are subjected to unitary transformations over reciprocal space, yielding generalized Wannier functions. While these functions are not inherently localized, localization is enforced by solving

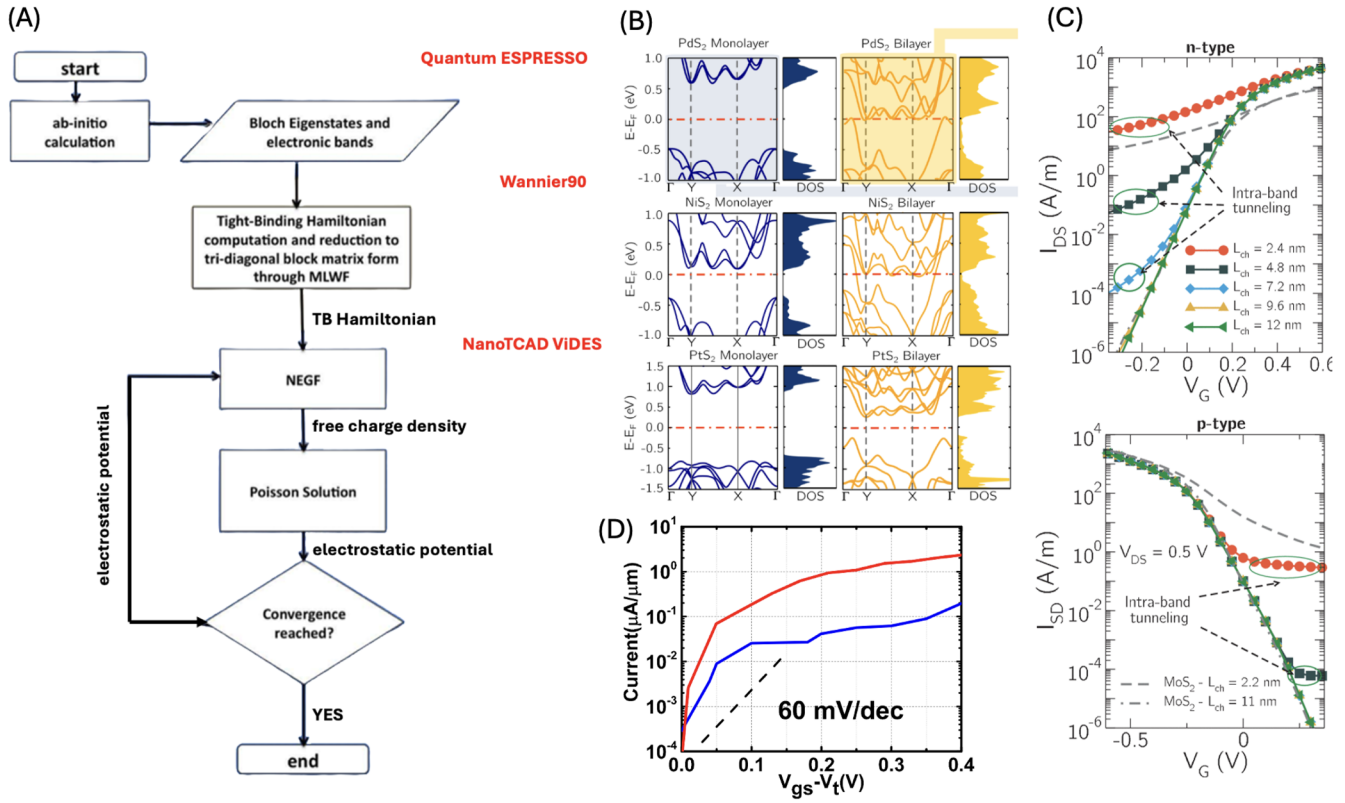


FIG. 5. (a) Flow chart of an open-source multi-scale framework for the simulation of nano-scale devices. Reproduced with permission from Bruzzone *et al.*, IEEE Trans. Electron Devices **61**, 48–53 (2014). Copyright 2014 IEEE. (b) Electronic band structure along a symmetric path in the Brillouin zone and DOS computed with DFT for monolayer and bilayer PdS_2, NiS_2, and PtS_2. Reproduced with permission from Marin *et al.*, ACS Nano **14**, 1982–1989 (2020). Copyright 2020 American Chemical Society. (c) Simulated transfer characteristics of the n-type (left) and p-type (right) InSe FETs for V_{ds} = 0.5 V and several channel lengths with t_{ox} = 0.5 nm and L_{ch} = L_g. MoS_2 FET characteristics (dashed lines) are included for comparison purposes. Reproduced with permission from Marin *et al.*, IEEE Electron Device Lett. **39**, 626–629 (2018). Copyright 2018 IEEE. (d) Simulated I_{DS}–V_{GS} curves for BP VTFET, a 3.3 nm long device with S/D doping (blue) and undoped D (red). From Lu *et al.*, *2017 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*. Copyright 2017 IEEE. Reproduced with permission from IEEE.

a function minimization problem. This process yields MLWFs that provide an effective tight-binding (TB) Hamiltonian for the electronic bands near the fundamental gap and facilitate efficient band interpolation. Elements within the TB Hamiltonians act as fitting parameters, allowing the calculation of carrier transport and charge distribution corresponding to each atom. Finally, the Hamiltonian with this basis of calculated MLWFs allows the calculation of current and transmission coefficients and properties such as electron and hole concentrations by the NEGF method (e.g., using NanoTCAD ViDES via a self-consistent NEGF and Poisson solver).

B. Comparisons of computational methodologies

While key computational tools and frameworks have been outlined in Sec. IV A, each comes with respective computational challenges: convergence issues, scalability, and accuracy vs computational cost. To reiterate, *ab initio* methods, particularly DFT, provide detailed insights into intrinsic material properties such as band structures, carrier dynamics, and electronic transport. These methods are critical for understanding the quantum-scale phenomena underlying TFET operation. However, they are computationally intensive and often impractical for simulating large, device-scale systems. The cubic scaling of DFT with the number of atoms imposes a significant computational burden, limiting its application to small-scale systems or simplified geometries. This poses a barrier to studying realistic nanodevices, particularly those involving long channel lengths, heterostructures, or large 2D material stacks.[82] Although recent advancements, such as linear-scaling DFT techniques, have demonstrated ways in improving efficiency, these methods often involve trade-offs in accuracy or require specific system properties to be effective.

TB models address some of the scalability issues of DFT by enabling faster simulations of larger systems. These models are particularly effective for exploring device-level characteristics, such as band alignment, tunneling probabilities, and current–voltage behavior. However, their accuracy is heavily reliant on the quality of empirical fitting parameters, which are typically derived from the experimental data or higher-level simulations.[83] This dependence brings challenges in predicting the behavior of novel materials or unconventional device architectures where such data might not be available or accessible. Furthermore, the transferability of TB models across different materials or operating conditions,[84] such as temperature or strain, remains a limitation that can reduce their predictive power. As we will see in Sec. IV C, ML-driven optimization shows promise in addressing these challenges to accelerate simulations but requires large datasets for training.

Gan *et al.* presented an example of a robust multi-scale simulation framework designed to address the computational challenges associated with *ab initio* methods, particularly the scalability issues of DFT.[85] The framework integrates DFT with tight-binding nonequilibrium Green's function (TB-NEGF) and Technology Computer Aided Design (TCAD) simulations to balance computational efficiency and accuracy. DFT, implemented using the NanoDCAL package, captures atomic-scale physics such as band alignment and carrier filtering mechanisms with high precision but is limited to systems of a few hundred atoms due to its cubic scaling with system size—which is mentioned precisely above. To overcome this limitation, this study uses calibrated Slater–Koster parameters derived from DFT to enable predictive TB-NEGF simulations, which extend the analysis to device-level systems involving over ten thousand atoms. This step significantly reduces computational costs while maintaining sufficient accuracy for device-scale predictions.

TCAD simulations are also employed to model realistic geometries and circuit-level performance using semiempirical parameters refined through DFT and TB-NEGF. This hierarchical approach ensures that key physics from atomic-scale simulations informs the design and optimization of large-scale systems. By integrating these methods, the framework addresses the bottlenecks of *ab initio* methods and demonstrates its effectiveness in simulating steep-slope silicon nanowire cold source FETs, achieving sub-60 mV/dec SS and high drive currents. The results highlight the potential of multi-scale frameworks to bridge the gap between material-level insights and device-level performance and could be a model for developing next-generation TFETs.

C. Applications of MS simulations

1. Graphene

Despite its lack of intrinsic bandgap, graphene has exceptional electrical properties that make it an interesting candidate for electronics. Fiori and Iannaccone[24] describe graphene-based transistors through MS modeling, presenting graphene nanoribbon (GNR) transistors,[86] graphene bilayer FETs,[87] and hexagonal boron-carbon-nitride (hBCN)/graphene heterostructures. The detailed MS approach helps overcome the limitations of graphene's zero bandgap through strategies such as bandgap engineering by chemical functionalization or the use of graphene in complex heterostructures. For GNR FETs, the simulations predict large I_{on}/I_{off} ratios for narrow devices, with performance strongly influenced by edge disorder and chemical modifications. These edge-related impacts were identified using atomistic simulations refined by tight-binding Hamiltonians derived from *ab initio* methods, effectively reducing computational costs while identifying mobility-limiting factors such as Anderson localization caused by edge defects.[24] The experimental validation of edge roughness impacts was demonstrated by Margani *et al.* in 2022,[88] who employed selective edge functionalization of graphene layers using 2-pyrone derivatives. They utilized Fourier Transform Infrared (FTIR) and Raman spectroscopy to characterize functionalized edge-specific chemical groups while maintaining basal plane integrity. While Margani *et al.* focused on functionalization's effects, their findings indirectly support simulation predictions of edge-induced impacts on transport properties, such as mobility degradation due to edge defects, as highlighted in the multiscale modeling by Fiori and Iannaccone.[24] More directly, Zhang *et al.*[89] provide experimental insights into GNR devices by showing how edge conditions influence tunneling transport in GNR TFETs. Their study demonstrated that precise control over GNR widths, ranging from 3 to 10 nm, enabled the tuning of energy bandgaps and minimized edge roughness-induced variability, supporting the need for edge-specific functionalization to achieve high on/off current ratios and low SS. This experimental work strengthens the link between computational models and real-world material performance by confirming edge-specific phenomena.

Graphene bilayer devices exhibit a bandgap modifiable by an external electric field, which is exploited in TFETs to achieve low-power operation suitable for digital applications. ML-driven optimization enhances these models by accurately capturing

band-to-band tunneling effects and enabling steep SS through the atomistic-level refinement of the band structure.[24] This predictive approach minimizes computational requirements while accurately identifying defect-related leakage mechanisms and enabling steep SS, leading to both cost reduction and defect identification. The graphene bilayer TFET has been explored in this way by others, mainly with Green's function theory.[90,91] In addition, hBCN can be innovatively used as a barrier material in graphene channels, effectively blocking band-to-band tunneling, leading to high I_{on}/I_{off} ratios and demonstrating the potential of 2D graphene in advanced electronics. By leveraging *ab initio* calculations to optimize tight-binding parameters, the MS approach reduces computational demands while accurately predicting transport behavior in hBCN/graphene heterostructures.[24] These simulations are, therefore, crucial for optimizing material synthesis and device architecture, by providing insights into quantum effects and the electrostatic properties of materials at different scales.

Zhang *et al.* have proposed and modeled a GNR TFET with the consideration of ribbon widths of 3–10 nm.[89] They show that a 5 nm ribbon width TFET has a low switching power of 0.1-V gate swing, and can theoretically achieve a 0.19 mV/dec SS. A low off-state current of 26 pA/μm was reported with a high on-state current of 800 μA/μm. Their results have been derived from a simplified analytical framework combined with the WKB approximation (see Sec. I) to project device performance.

While Zhang *et al.* demonstrate GNR's potential through a simplified framework, Lv *et al.* confirm their findings through the MS-approach.[92] They have investigated a segmented edge saturation (SES) GNR TFET through a multi-scale simulation approach combining aforementioned DFT and NEGF methods. DFT simulations, conducted using Quantum ESPRESSO, calculated edge saturation effects for hydrogen (H), fluorine (F), and hydroxyl (OH) on armchair GNRs (aGNRs) with ribbon widths ranging from 7 to 27 carbon atoms. The optimized bandgaps (E_g) of OH- and H-saturated GNRs in the 3m + 1 family were selected for the device, with tunneling and blocking segments exhibiting E_g values of 0.48 and 0.93 eV, respectively. The device simulations employed NanoTCAD ViDES with a refined tight-binding model, incorporating updated parameters to account for saturation-induced band structure variations, reducing errors by 90% compared to traditional TB parameters. The double-gate structure featured a GNR width of 1.5 nm, a channel length of 20 nm (8 nm OH-saturated and 17 nm H-saturated regions), an oxide thickness equivalent to 1 nm of SiO_2, and a supply voltage of 0.4 V. Transport simulations used a grid resolution of less than 1 Å and an energy resolution of 1×10^{-3} eV, ensuring the accurate detection of confined states within a few meV. By iteratively solving Schrödinger's and Poisson's equations, the SES GNR TFET demonstrated the feasibility of leveraging edge saturation to tailor electronic properties.

A more recent study from Vobulapuram *et al.* in 2023 reported to have designed and modeled a bilayer graphene nanoribbon TFET (BLGNR-TFET) using the QuantumATK 2018.06 simulation platform.[93] The parameter, n, is used for the dimer line number, calculating different bandgaps for different n values. This is due to GNR acting as either a semiconductor or a conductor depending on the number of carbon atoms present across the GNR widths. The device incorporates a dual-gate architecture with a 20 nm armchair GNR channel of $n = 10$, a 1 nm SiO_2 dielectric, and a GNR sheet thickness of 0.33 nm. The device structure uses a p^+-doped source and n^+-doped drain regions, each 10 nm long, with the central intrinsic region forming the channel. The simulations employ the extended Hückel basis set and self-consistent DFT with the NEGF formalism. The sampling parameters for the k-grid are $k_a = 1$, $k_b = 1$, and $k_c = 100$, while the density mesh cutoff is set to 10 hartree. The simulations are conducted at 300 K. The BLGNR-TFET achieves improved transconductance and drain current compared to monolayer GNR-TFETs (MLGNR-TFETs), with a maximum drain current of ~7 μA at $V_{GS} = 2$ V. These results show ballistic transport in the channel and high transconductance, underlining the potential of BLGNR-TFETs for low-power and high-performance applications in VLSI circuits. As such, MS simulations have aided to establish a direct relationship between electronic structure and device efficiency.

This is particularly significant, as no experimental reports to date have demonstrated GNR or graphene bilayer TFETs achieving subthermal SS, despite theoretical studies and simulations predicting their potential. A key challenge lies in the exponential dependence of SS on temperature, which causes substantial degradation in subthreshold characteristics at room temperature.[28,94] In addition to an unacceptably large SS, the room-temperature performance of reported GNR-TFETs is further compromised by their exceedingly small on-state/off-state current ratio.[95] This stems from GNR's small bandgap, which leads to significant leakage currents in the off-state and limits the contrast between the on and off states. The insufficient bandgap also hinders tunneling efficiency, reducing the achievable drive current in the on-state. There are also significant challenges in the patterning and processing of GNRs that limit experimental realization. Current fabrication methods face significant challenges in achieving nanoribbons with precise edge structures and uniform widths, of which both are required for achieving the required bandgap and minimizing edge scattering effects. Variability in ribbon dimensions due to processing inconsistencies further degrades device performance and limits reproducibility. These factors, therefore, also highlight the need for novel fabrication methods to address these issues and allow the potential of GNR-TFETs to be realized in practical applications.

2. TMDs

MoS_2 TFET devices are also being investigated as a promising TMD for TFET applications, with numerous MS simulation studies supporting this research. Marian *et al.*[96] contribute to this body of work by using MS simulations to introduce two advanced transistor concepts based on lateral heterostructures within a monolayer of MoS_2 that integrates adjacent metallic (1T) and semiconducting (2H) phases. These concepts are highly regarded for application in both high-performance and low-power devices. This paper discusses a lateral-heterostructure (LH) TFET with a semiconducting MoS_2 channel sandwiched between metallic MoS_2 regions, designed for superior electrostatic control and operating efficiency. A second concept is the planar barristor—a laterally gated Schottky diode—which effectively connects a metallic source to a semiconductor drain. The LH FETs feature a near-ideal SS of 69–100 mV/dec over various channel lengths (Table II), providing excellent electrostatic control for high-performance applications. They also exhibit impressive I_{on}/I_{off} ratios that not only exceed 10^4 for high-performance requirements but also exceed 10^6 for low-power

TABLE II. Figures of merit for different channel lengths of the LH FET and DG planar barristor using monolayer MoS_2 for HP and low-power (LP) applications. Reproduced with permission from Marian *et al.*, Phys. Rev. Appl. **8**, 054047 (2017). Copyright 2017 American Physical Society.

		High performance					Low power			
		SS (mV/dec)	I_{on}/I_{off}	τ (ps)	PDP (fJ/μm)	f_T (THz)	SS (mV/dec)	I_{on}/I_{off}	τ (ps)	PDP (fJ/μm)
LH FET (V_{DS} = 0.6 V)	L_{ch} = 3.3 nm[a]	102	1.0×10^4	0.16	0.10	3				
	L_{ch} = 5.5 nm	69	1.18×10^4	0.22	0.16	2	72	4.38×10^6	0.44	0.12
	L_{ch} = 6.6 nm	69	1.20×10^4	0.25	0.18	1.5	70	4.43×10^6	0.49	0.13
	L_{ch} = 8.27 nm	69	1.23×10^4	0.30	0.22	1.4	68	4.65×10^6	0.47	0.13
	L_{ch} = 9.9 nm	69	1.25×10^4	0.35	0.26	1.0	69	4.41×10^6	0.61	0.16
Planar barristor (V_{DS} = 0.4 V)	DG	68.5	9.8×10^3	0.14	0.055	3	72.5	3.5×10^5	1.2	0.017
	SG (t_{oxb} = 0.5 nm)	73	4.4×10^3	0.16	0.028	2.8	79	1.5×10^5	1.8	0.011
	SG (t_{oxb} = 5 nm)	79	3.7×10^3	0.2	0.029	2.3	85	7.4×10^5	4.4	0.013

requirements with channel lengths of at least 5.5 nm. In parallel, the planar barristor, especially in its double-gate configuration, exhibits SS values below 79 mV/dec, reflecting its gating efficiency. Its on/off ratio approaches 10^4, reinforcing its potential as a formidable competitor to conventional CMOS technology. These results, which encapsulate the devices' switching capabilities and mastery of off-state current leakage, suggest that MoS_2-based lateral heterostructures hold great promise for the next generation of transistor technology, marking a step forward in the quest for devices that balance high performance with low-power consumption.

The transport properties of monolayer and bilayer configurations of PdS_2, PtS_2, and NiS_2 were also calculated [Fig. 5(b)].[47] The results from Marin *et al.*[47] indicate that LH-FETs fabricated with NiS_2 do not meet the ITRS benchmarks due to its minimal bandgap and inherent ambipolar characteristics. However, LH-FETs fabricated with PdS_2 and PtS_2 meet the IRDS performance criteria, demonstrating their potential for integration into future high-performance digital applications. These results confirm the potential of 2D-based FETs beyond graphene to transcend the subthermal limit, thus inviting further research into 2D materials with more acute DOS and lower SS. In particular, noble TMDs have been instrumental in achieving subthermal SS in FETs under ambient conditions, mainly due to their distinct DOS properties.

The insights provided by these MS simulations help researchers and device designers by providing a predictive benchmark against which to measure and refine their fabrications. This predictive capability not only provides information on expected transfer characteristics but also outlines the underlying physical principles that govern device behavior, which is critical to the design of advanced semiconductor devices. For example, InSe, with its high mobility and favorable bandgap of about 1.5 eV,[97] is emerging as an ideal candidate for the fabrication of ultrathin digital electronics. For n-type FETs, an SS of 65 mV/dec and an I_{on}/I_{off} ratio greater than 2.7×10^4 were predicted for devices with a channel length of 7.2 nm.[81] These transfer characteristics from Marin *et al.*, as seen in Fig. 5(c), indicate strong potential for high-performance applications, while also pointing to significant source-to-drain tunneling effects in shorter channels.[81] This is an important consideration for future device miniaturization. The p-type FETs exhibit less tunneling due to the larger effective hole mass, enabling robust performance at channel lengths greater than 7.2 nm. The improved performance of InSe FETs, despite their sensitivity to variations in oxide thickness, particularly in p-type devices, and their stability against gate length variations—with minimal performance degradation even at 30% gate underlap—provide practical insights into the fabrication of consistent and reliable transistors. These InSe FETs not only outperform MoS_2 nFETs in terms of on-current and on–off ratio but also exhibit greater robustness against intraband tunneling, a critical advantage over MoS_2 pFETs. Such transfer characteristics provide experimentalists with concrete performance benchmarks to aim for, thus influencing the trajectory of future experimental efforts.

There have been notable experimental demonstrations of successfully fabricated TMD-based TFETs. In 2015, Sarkar *et al.* introduced a subthermionic TMD-based TFET, termed the ATLAS-TFET, which utilized an ultra-thin bilayer MoS_2 channel of 1.3 nm thickness and degenerately doped p-type Ge as the source.[98] This device achieved a remarkable minimum SS of 3.9 mV/decade and an average SS of 31.1 mV/decade over four decades of drain current at room temperature, operating at an ultra-low drain–source voltage (V_{DS}) of 0.1 V. The high on/off current ratio was attributed to the staggered heterojunction between Ge and MoS_2, which enabled efficient BTBT. This study utilized analytical modeling combined with electrostatic simulations to design the heterostructure and predict the tunneling mechanisms that contributed to its exceptional performance. More recently, in 2020, Oliva *et al.* experimentally demonstrated a vertical $WSe_2/SnSe_2$ heterojunction TFET with subthermionic performance.[99] This device achieved a minimum SS of 35 mV/dec at V_{DS} = 500 mV at room temperature, maintaining an exceptional on/off current ratio exceeding 10^5 and an off-state current below 0.1 pA/μm^2. This study incorporated DFT calculations using the Vienna *Ab initio* Simulation Package (VASP) to model the band alignment, confirming a type III broken-gap heterojunction alignment critical for efficient BTBT. These experimental results validate the promise of TMD material systems and their theoretical modeling in advancing the development of high-performance, energy-efficient TFETs.

3. Black phosphorous

The BP-based TFET device is noteworthy for its potential in achieving ultra-scaled, low-power, and steep subthreshold logic devices due to the excellent electrostatic control afforded by 2D materials' narrow thickness. MS simulations employing a quantum simulation framework on BP TFET devices in diverse structural configurations (including heterojunction and homojunction arrangements) and varying chemical doping concentrations facilitate the optimization of device design and energy-delay metrics. The simulations indicate that tri-layer BP TFETs exhibit remarkably high on-currents in comparison with tri-layer WTe_2 DG TFETs.[100] This performance is attributed to the superior material properties of tri-layer BP, namely a smaller effective mass and a larger transverse effective mass, which enhance the transmission probability and on-state current. In addition, the bandgap of the tri-layer BP (E_g = 0.76 eV) contributes to this effect. The device structure of this study also included an interfacial layer (IL) between the dielectric and the two-dimensional material. This resulted in an increase in the on-current by three to four times its original value and served to mitigate the limiting effects of fringing fields at the source channel junction. Thus, the device performance can be significantly enhanced by effectively reducing the tunneling distance and shaping the potential distribution to be steeper at the junction.

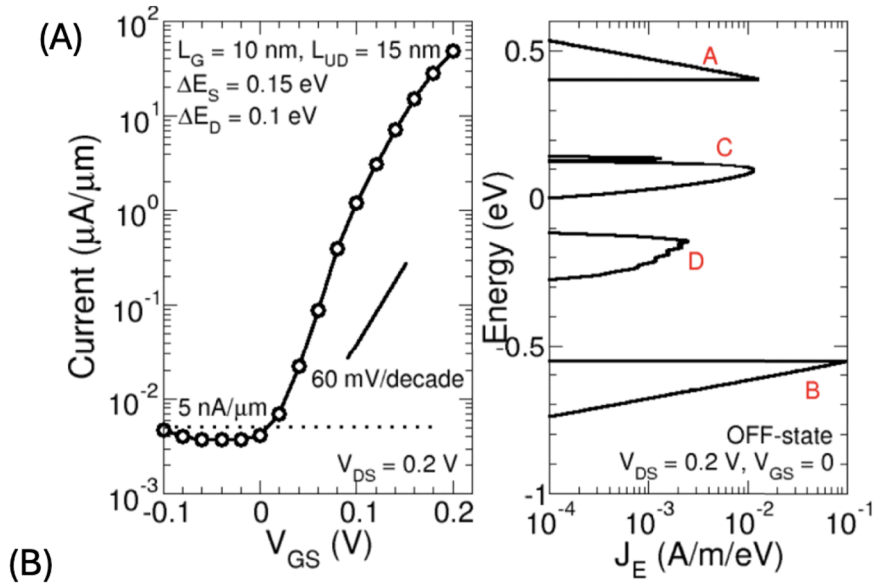
Moreover, MS simulations provide a means of conducting energy-delay analysis, thereby enabling the assessment of a range of off-currents and supply voltages. Such evaluations demonstrate that tri-layer BP TFETs can maintain energy efficiency in comparison with monolayer BP FETs. The energy-delay product analysis demonstrated that for a target off-current (I_{off}) of 10^{-5} μA/μm, the tri-layer BP TFETs exhibited superior delay and energy-delay product (EDP) characteristics across a range of supply voltages (V_{DD}), particularly outperforming monolayer BP FETs at supply voltages below 0.5 V.[100] It is, therefore, evident that the capacity to undertake simulations that encompass a range of scales is of paramount importance to the advancement and innovation of TFET technologies. Such simulations provide a framework for predictive modeling and design, enabling the resolution of current challenges and the guidance of future advancements within this field. This study demonstrated the promising results of tri-layer BP TFETs using the proposed device design with IL, which exhibited a superior performance compared to existing 2D FETs at lower supply voltages. Furthermore, the utility and efficiency of the MS simulations employed underscore the significance of advancing the functionality and innovation within TFET technologies.

Lu *et al.* also examined the utilization of BP for vertical TFET devices with asymmetric layer numbers for the top and bottom layers and an undoped drain by employing MS simulations.[68] Moreover, the impact of varying the number of layers in the source material is examined, along with device performance with and without chemical doping. The results [as seen in Fig. 5(d)] demonstrated that the SS and on/off current ratio for this device structure can be maintained below 10 mV/dec and beyond 10^5, respectively, when the channel length is reduced to 3 nm [Fig. 5(d)]. Even at a channel length of 3.3 nm, the device exhibits a relatively low SS of ~6 mV/dec, demonstrating a lesser degree of degradation in SS and on/off ratio in comparison with devices with conventional source/drain doping.[68] The design exploits the layer-dependent properties of BP and its exceptional electrostatic control, which extends to the off-state, a crucial aspect for ultra-short channel TFETs aiming to minimize off-current while optimizing device performance. It was observed that for channel lengths below 10 nm, the use of an undoped drain can result in enhanced device performance, while an increase in on-current can be achieved by increasing the number of layers in the source. Furthermore, the on-current can be increased by another order of magnitude through the implementation of alterations in the channel orientation, specifically from zigzag to armchair.

In 2020, Kim *et al.* experimentally demonstrated BP-based natural heterojunction TFETs (NHJ-TFETs) with spatially varying BP layer thickness, achieving an exceptional device performance.[70] The fabricated devices utilized bulk BP as the source and monolayer BP as the channel and drain regions. By leveraging the layer-dependent bandgap of BP and the absence of interface defects typical in conventional heterojunctions, the NHJ-TFETs achieved a record-low average SS ($SS_{ave,\ 4dec}$) of 22.9 mV/dec over four decades of current and a $SS_{ave,\ 5dec}$ of 26.0 mV/dec over five decades at room temperature. The devices also demonstrated high I_{60} values of 0.65–1 μA/μm and excellent on/off current ratios exceeding 10^5. Notably, the NHJ-TFETs exhibited temperature-independent SS_{ave} in the band-to-band tunneling regime, confirming the dominance of BTBT as the carrier injection mechanism. These results validate BP's potential for developing high-performance, low-power TFETs while addressing the limitations of traditional heterojunction interfaces.

4. Newly found 2D materials

Group-V materials, renowned for their uniquely buckled honeycomb configurations such as As-ene, Sb-ene, and bismuth-ene (Bi), have been identified as promising candidates for TFET design owing to their ambient stability and small effective masses, as outlined by Kanungo *et al.*[28] in their study on nanoscale TFETs. Among these, Bi is particularly distinguished for its minimal and direct energy bandgap. The crystal structure of Bi_2Se_3 is rhombohedral with a nominal direct energy bandgap. Zhang *et al.*[62] utilized *ab initio* simulations to assess a Bi_2Se_3 thin film, revealing a bandgap of 0.252 eV and positing its utility as a TFET channel material optimized for low-power logic applications. This material exhibited a subthermal SS over 4 orders of magnitude of 50 mV/dec at V_{DS} = 0.2 V [Fig. 6(a)] and a robust I_{on}/I_{off} ratio under minimal supply voltage, an advance reported by Zhang *et al.*[62] Furthermore, Li *et al.* extended *ab initio* simulations to assess the wider spectrum of group-V materials—As, Sb, and Bi—and their deployment in 10 nm gate-length TFETs [Fig. 6(b)].[101] Monolayer bismuthine emerged with the highest on-state current, satisfying the ITRS benchmarks for high-performance devices. In addition, these group-V material-based TFETs showcased considerably reduced delay times and power dissipation, compared to ITRS standards. Among the hexagonal monolayer group V-ene contenders, the monolayer Bi TFET was identified by Li *et al.* as offering superior device performance in terms of on-state current, delay time, and power dissipation for high-performance applications.[102] In addition, the monolayer Sb TFET demonstrated a favorable performance, ranking closely behind the Bi TFET. These investigative simulations extend to the domain of MOSFET performance, wherein the aforementioned materials also exhibit considerable promise. Pizzi *et al.* employed MS simulations to examine As- and Sb-based MOSFETs, and their



		I_{on} (μA μm^{-1})	I_{min} (μA μm^{-1})	Min SS (mV/dec)	Avg SS (mV/dec)	C_g (fF μm^{-1})	τ (ps)	PDP (fJ μm^{-1})
Arsenene	HP	101	$\sim 10^{-8}$	55	244	0.026	0.11	0.17
	LP	63	$\sim 10^{-8}$	55	114	0.026	0.302	0.035
Antimonene	HP	173	$\sim 10^{-8}$	50	228	0.01	0.067	0.103
	LP	97	$\sim 10^{-8}$	50	111	0.01	0.074	0.033
Bismuthene	HP	1153	$\sim 10^{-2}$	96	182	0.008	0.005	0.032
Bismuthene NCTFET	HP	1868	$\sim 10^{-2}$	78	145	0.020	0.008	0.090
WTe_2	HP	240	$\sim 10^{-8}$	39	221	0.052	0.159	0.133
	LP	141	$\sim 10^{-8}$	39	108	0.052	0.27	0.072
BP	HP	2422	$\sim 10^{-2}$	58	169	0.081	0.025	0.05
ITRS	HP	1450	—	—	178	0.93	0.475	0.51
	LP	461	—	—	98	1.0	1.562	0.52

FIG. 6. (a) Left: Transfer characteristic of the n-type 2QL Bi_2Se_3 TFET at $V_{DS} = 0.2V$ and room temperature, showing an effective SS of 50 mV/decade over 4 orders of magnitude. Right: Current spectrum in the off-state, demonstrating effective management of all four leakage components. Reproduced with permission from Zhang *et al.*, IEEE Electron Device Lett. **35**, 129–131 (2014). Copyright 2014 IEEE. (b) Benchmark comparison of ballistic device performances of ML group V-ene TFETs and ML bismuthene NCTFETs for high-performance (HP) and low-power (LP) applications, matched against the ITRS 2013 requirements. Also includes performance data for the ML WTe_2 TFET and ML BP TFET. Reproduced with permission from Li *et al.*, Semicond. Sci. Technol. **34**, 085006 (2019). Copyright 2019 IOP Publishing.

findings indicated that ITRS benchmarks were met, thereby supporting the possibility of utilizing these valuable theoretical insights for further experimental research on these materials.[103]

V. MACHINE LEARNING METHODS

While MS simulations offer comprehensive insights by modeling physical phenomena at scales ranging from atomic to device levels, they are not without significant limitations.[104] The integration of quantum mechanical models into MS simulations places a considerable computational burden on the system, which is a necessity for TFETs. This can present a significant challenge to the rapid iteration of devices.[79] Furthermore, integrating simulations across quantum and classical regimes introduces additional complexity due to the disparate physical models and assumptions inherent to each domain.[105] In instances where high-throughput screening of materials and design parameters is necessary, the computational burden associated with MS simulations represents a significant challenge. Furthermore, the identification of anomalies, such as material defects, is not a straightforward process and frequently necessitates the implementation of extensive simulation customization. The application of ML methods offers a promising avenue for addressing these challenges. They are capable of processing intricate datasets and delivering predictions with greater expediency than MS simulations. In other words, they are capable of modeling high-dimensional spaces in a more efficient manner than MS simulations.

With sufficient training, ML algorithms are capable of identifying intricate patterns and relationships in data that are beyond the computational capabilities of MS simulations.[106] Another notable advantage of ML is its scalability,[107] which enables the handling and analysis of vast amounts of data with greater efficiency than MS simulations. This is particularly advantageous when investigating novel TFET materials and structures, where the design space can be extensive.

Deep learning (DL) is a high-dimensional method and a subset of ML that employs numerous layers and parameters.[108] In contrast, ML methods such as support vector machines (SVMs), random forests (RFs), and gradient boosting machines (GBMs) are lower-dimensional models that serve as data science tools rather than performance prediction methods. They can ingest large datasets and contribute to the design aspects of TFETs, specifically by sifting through various design parameters and effects of device performance to prioritize the parameters that should be of focus. This can assist in streamlining the design process of these devices; however, these methods are not as powerful as DL in predicting device performance. Consequently, ML methods are increasingly becoming essential tools in the TFET domain. They facilitate the acquisition of more rapid, scalable, and frequently more intricate insights into device performance, thereby offering a valuable addition to the insights provided by traditional MS simulations. This section will summarize the essential ML techniques pertinent to TFETs, highlighting their role in enhancing the efficiency and effectiveness of TFET design and performance prediction (Table III).

A. Artificial neural networks (deep learning)

The application of neural networks, a technique used within DL, represents an optimal approach to the design of TFETs, facilitating the optimization of both TFET architectures and materials. Such techniques are effective in forecasting performance metrics, including on/off ratios and SS. Artificial neural networks in DL are computational models that emulate the structural organization of the brain's neural networks.[109] These networks are composed of interconnected layers of nodes that process and relay information. They are particularly noteworthy in the field of computational modeling. A typical network comprises three layers: an input layer, multiple hidden layers, and an output layer.[110] Each node within the network assigns weights to inputs and utilizes an activation function to generate an output. DL is particularly adept at processing complex data, such as images, due to its ability to learn diverse data features at varying levels of complexity through its multiple layers.[111] In the context of TFETs, neural networks demonstrate a particular aptitude for discerning how alterations in design may influence device performance. This is achieved through the analysis of data pertaining to material types, geometries, and other design parameters. Methods such as RF, GBMs, and SVMs are effective at identifying which parameters are most influential in a TFET's design, thereby guiding the prioritization of design strategies. However, they may not fully capture the range of complexities involved in performance prediction with the same efficacy as DL. Conversely, DL networks are capable of optimizing design parameters by identifying patterns within the data and making accurate predictions about device performance. This dual capability is due to their ability to abstract different levels of features from raw data, learn from them, and make predictions based on a deep understanding of the underlying relationships.[112] Consequently, neural networks serve as a comprehensive tool for TFET development, offering advantages in both optimizing design parameters and predicting device performance with a higher degree of sophistication and accuracy than their lower-dimensional counterparts.

Wang *et al.* employed DL to address the limitations of Si-TFETs, namely low on-state currents and significant ambipolar leakage.[113] They achieved this by proposing a GeSi/Si heterojunction double-gate TFET with a T-channel hetero-gate dielectric structure. The DL model was able to achieve high predictive accuracy and re-emphasizes the opportunity to predict performance from given design parameters in a more efficient and direct optimization process. Furthermore, this model incorporated both forward and

TABLE III. Comparison of common ML methods and their suitability for TFET design and/or prediction.

	Neural networks	GBMs	RFs	SVMs
Pros	Model high-dimensional spaces. Complex pattern recognition and prediction	Iteratively refine predictions. Good for subtle influences in performance	Handle various data types. Good for categorization. Less prone to overfitting	Generalize well. Avoid overfitting. Good for small/medium datasets
Cons	Require substantial training data. Computationally expensive. Need expert tuning	More prone to overfitting. Require careful tuning. Computationally intensive	Sensitive to changes in the training set. Less efficient with high-dimensional data	Binary. Ineffective for multi-class problems. Struggle with large datasets
TFET suitability	Suitable for modeling the nonlinear and high-dimensional characteristics of TFETs, including physical effects and device behavior	Well-suited for identifying and optimizing key TFET parameters with subtle influences on performance	Useful for categorizing TFET performance trends but less effective for detailed modeling of high-dimensional data	Best for binary classification tasks in TFET design, such as distinguishing operational states, but limited for broader design predictions

inverse design principles, which suggest optimal device structures based on targeted performance goals. This enables custom TFET engineering for devices with specific applications.

In a recent study, Choudhary *et al.* employed an ML technique, the Atomistic Line Graph Neural Network (ALIGNN), in conjunction with DFT for the design of 2D van der Waals heterostructures.[114] A total of 674 non-metallic two-dimensional materials were subjected to analysis, with the objective of creating 226 779 potential heterostructures. The results yielded insights into the most prevalent types of heterostructures, which were identified as type II and type III, the least common. This approach enabled the extraction of insights into chemical trends and potential applications in photocatalysis and high work function metal contacts for devices. Consequently, the deployment of ML tools to predict band alignment information can markedly accelerate the material selection process for device applications. The integration of ML in this context reiterates the accelerated development of device design and optimization, and how it can also enable a more targeted exploration of a vast device design space for 2D materials.

Inspired by physical principles, Li *et al.* put forth a neural network methodology, for modeling TFET devices.[115] This method addresses the limitations of traditional multilayer perceptron (MLP) neural networks, which often fail to incorporate the physical principles that govern the device's operation, resulting in models that exhibit unphysical behavior. In contrast, physics-inspired neural networks (Pi-NNs) assure the precision and efficacy of generated models by integrating the fundamental physics of the TFET device into its neural network architecture. This is accomplished by processing disparate input variables through discrete sub-networks, which are configured to reflect particular physical effects on device performance. To illustrate, the method proposed by Li *et al.* employs tanh and sigmoid activation functions in various network components to emulate the physical response of TFETs to alterations in drain–source voltage (V_{DS}) and gate voltage (V_{TG}).[115] This is demonstrated by the model's ability to ensure that the current is equal to zero when V_{DS} is equal to zero, which illustrates a well-behaved I_D–V_{DS} relationship around $V_{DS} = 0$ and excellent subthreshold region fitting (see Fig. 7). This approach facilitates the generation of more refined and precise transfer characteristics (I–V curves) from discrete data points, while simultaneously reducing the complexity of the underlying model. The Pi-NN method from Li *et al.* employs a relatively smaller number of parameters (7 neurons and 20 parameters in total), thereby prioritizing enhanced computational efficiency and performance. While this configuration is relatively small compared to typical deep learning models, which often involve numerous layers and thousands of parameters, it demonstrates the potential of compact neural networks for specific tasks. That is, it has the potential to facilitate more rapid and reliable design and optimization of TFETs and other electronic devices by integrating the depth of physical modeling with the flexibility of ML approaches.

Wu and Guo presented an ML-based framework that employs DL with the objective of streamlining quantum device simulations, with a particular focus on ferroelectric tunnel junctions (FTJs).[116] The results demonstrated the efficacy of the DL technique in reducing the feature size of device properties while maintaining a sparse representation, thereby retaining key information. Regression algorithms, specifically kernel ridge regression, show high prediction accuracy with a small training dataset. The framework's computational efficiency is evidenced by a prediction speed that is 10 000 times faster than that of NEGF simulations. The methodology included employing DL for dimensionality reduction, implementing regression algorithms to establish parameter-property mapping, and refining the relationship through feature engineering. It illustrates how applying ML model holds superiority over MS simulations. Nevertheless, in comparison with the Pi-NN model, the integration of fundamental physics into ML models results in a more expeditious and efficacious design and optimization of TFET technology.

B. Other ML methods

1. Support vector machines

Among the ML methods discussed, SVMs are distinguished by their relative simplicity.[117] The principal objective of this method is to identify a hyperplane within a multidimensional space that can effectively segregate data points into distinct categories.[118] SVMs are particularly well-suited to small- and medium-sized datasets, as they are highly effective at producing models that generalize well and avoid overfitting when tuned correctly. It should be noted, however, that the process of proper tuning can present a significant challenge. SVMs are inherently designed for binary classification, which can render them less practical for multi-class problems that require supplementary techniques. In the context of TFET design, SVMs are particularly effective when the data relationships are evident and the design landscape is more comprehensible. However, their limitations become apparent when confronted with large datasets or tasks that necessitate navigation through complex, high-dimensional data spaces.[118] Given their relative simplicity in comparison with deep learning and other advanced machine learning approaches, SVMs are recommended for use in the preliminary phases of the TFET design process. They provide a robust foundation for preliminary exploration of the design space, offering a more straightforward computational alternative before transitioning to more sophisticated, computationally intensive models for further refinement.

Murugathas *et al.* employed SVMs to predict the performance parameters of carbon nanotube (CNT) bundle network FETs under liquid-gated conditions.[119] A total of 119 devices were examined to explore the role of CNT junctions in electrical conduction and gating. The input parameter was the CNT bundle density, which was measured using atomic force microscopy (AFM) images. The target parameters were the on/off current and threshold voltage of FETs [see Figs. 8(a)–8(c)]. The on-current was predicted with greater than 90% accuracy, while the off-current and threshold voltage were predicted with ~82% and 77% accuracy, respectively. Correlation issues and inaccuracy were observed, which were affected by other parameters, such as network composition. Nevertheless, the effectiveness of SVMs in predicting electronic parameters was demonstrated, despite these issues. It should be noted that SVMs were able to achieve good results in this study due to the presence of strong correlations in the dataset, specifically between on-current and CNT bundle density. However, the accuracy of the model was found to be significantly influenced by even slight variations and complexities in the data.

In another study, Bian *et al.* employed SVMs and CNT to develop a carbon nanotube-based FET (NTFET) decorated with

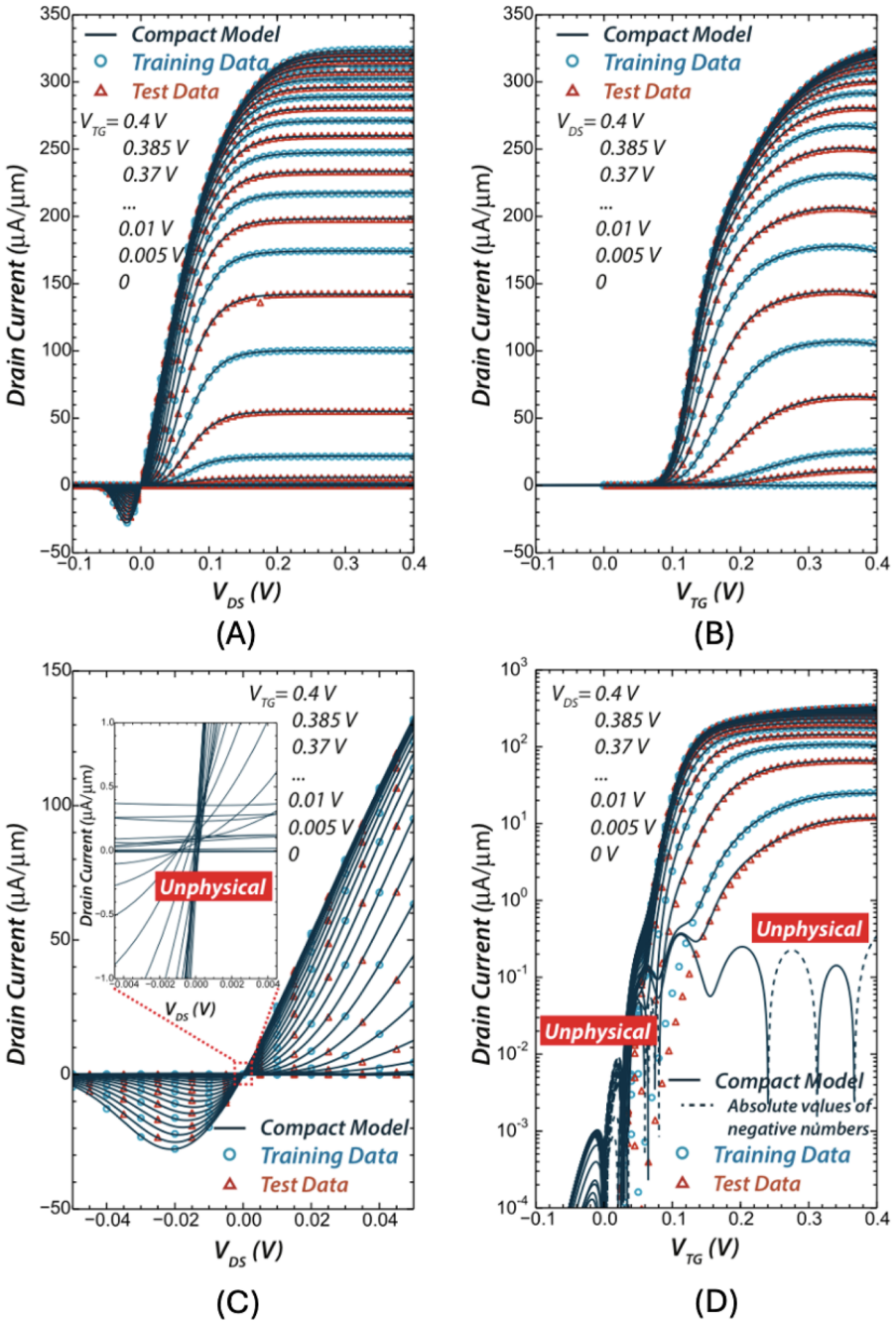


FIG. 7. (a) I_D vs V_{DS} at different V_{TG} values. (b) I_D vs V_{TG} at different V_{DS} values in linear scale. (c) I_D vs V_{DS} at different V_{TG} values around V_{DS} = 0; the embedded plot shows unphysical I_D–V_{DS} relationships around V_{DS} equals 0. (d) I_D vs V_{TG} at different V_{DS} values in semilog scale; unphysical oscillation of ID around zero appears in the subthreshold region and when V_{DS} = 0. Reproduced with permission from Li *et al.*, IEEE J. Explor. Solid-State Comput. Devices Circuits **2**, 44–49 (2016). Copyright 2016 IEEE.

metal nanoparticles for the detection and discrimination of purine compounds.[120] By applying SVMs and linear discriminant analysis ML methods to the NTFET data, they demonstrated a 93.4% accuracy rate with a reduced feature set of only 11, which outperformed the 95% accuracy achieved through a linear discriminant analysis with 48 features. The NTFET characteristics of transconductance, threshold voltages, and minimum conductance were identified as the primary sensing descriptors for classification. Xu *et al.* presented another example of the use of SVMs for the modeling of SiC based metal–semiconductor FETs, which comprise a cap layer, a channel layer, and a buffer layer on a 4H-SiC substrate.[121] The input parameters were the gate–source voltage, the drain–source voltage, and the operational frequency. The output parameters were the S-parameters. The SVMs demonstrated satisfactory accuracy in predicting FET performance, as evidenced by Mean Squared Error (MSE) values in the range of 1.83×10^{-5} to 2.60×10^{-3} and

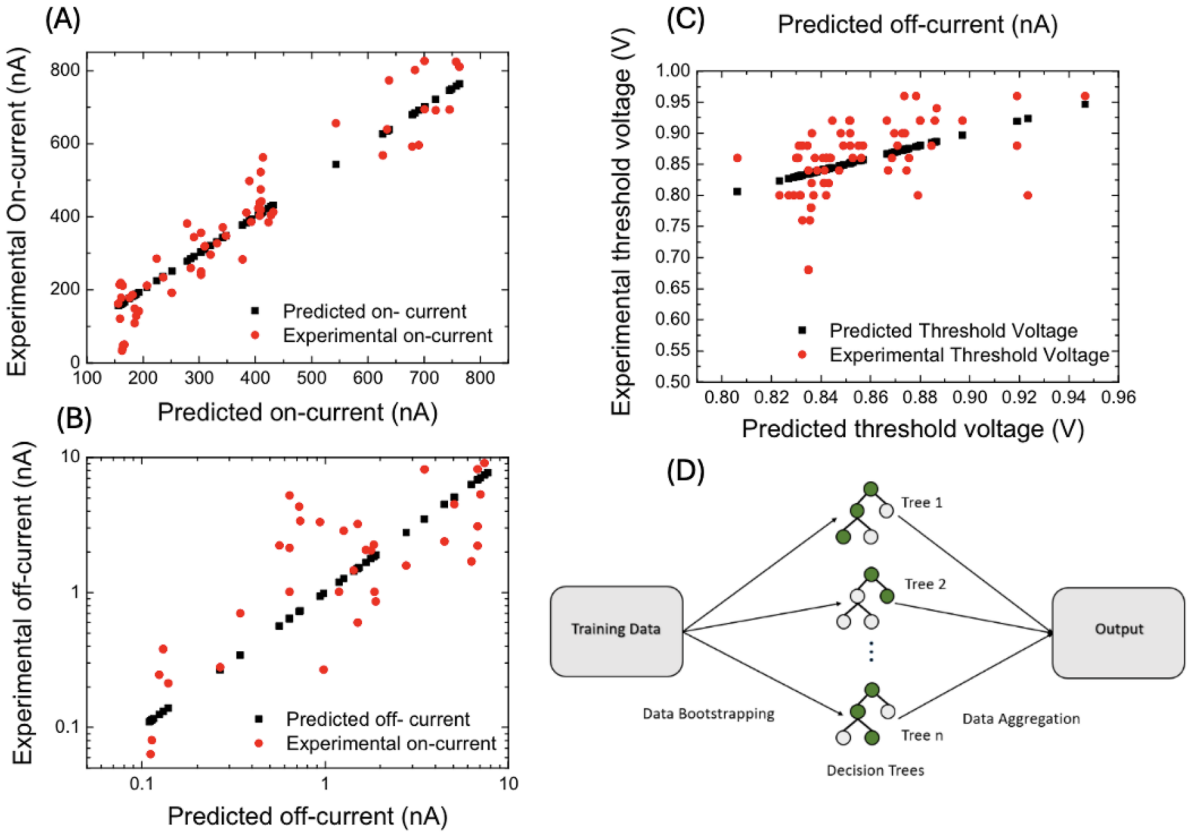


FIG. 8. Comparison between the observed and predicted values of (a) on-current, (b) off-current, and (c) threshold voltages of liquid gated CNT network FETs by the SVM model. From Murugathas *et al.*, *2022 IEEE International Conference on Nanoelectronics, Nanophotonics, Nanomaterials, Nanobioscience and Nanotechnology (5NANO)*. Copyright 2022 IEEE. Reproduced with permission from IEEE. (d) Schematic representation of the working of a random forest algorithm. From Nirosha *et al.*, *2023 International Conference on Recent Advances in Electrical, Electronics, Ubiquitous Communication, and Computational Intelligence (RAEEUCCI)*. Copyright 2023 IEEE. Reproduced with permission from IEEE.[126]

correlation coefficient (R) values from 0.971 to 0.997 for the training dataset and R values from 0.915 to 0.991 for the testing dataset.[121]

For TFET design, the aforementioned implications reinforce the suggestion that SVMs be employed for the initial stages of TFET design, particularly for tasks such as feature selection and the optimization of design parameters. The model's capacity to operate with a more condensed feature set while maintaining high accuracy makes SVMs an attractive option for streamlining the design process.

2. Random forest

RF regression (RFR) is a ML method particularly well-suited to the dimensionality of TFET design parameter optimization, as opposed to performance prediction. RFR functions by constructing a multitude of decision trees during the training phase and subsequently aggregating their predictions. The method's resilience to overfitting and versatility with different types of data make it an ideal tool for identifying which parameters are most crucial in the TFET design process. It has been demonstrated to be applicable to a diverse range of prediction problems with a limited number of parameters to be tuned, and it is suitable for smaller datasets and high-dimensional feature spaces for categorization.[122–124] However, it has been observed to be sensitive to minor alterations in the training dataset and may be less resilient to overfitting than GBMs.[125] This method is highly adept at understanding the manner in which various design parameters influence key performance metrics, including on/off current ratios and threshold voltages. Nevertheless, RFR, in conjunction with SVMs and GBMs, is best utilized for the prioritization of design alternatives. These data science tools, while formidable, do not rival the predictive capacity of deep learning models and are recommended for the guidance of design rather than the prediction and optimization of device performance.

In a recent study, Nirosha *et al.* employed a RF model [Fig. 8(d)], to assess the role of contact resistance (Rc) in organic thin film transistors (OTFTs). Subsequently, they optimized the prediction of Rc behavior.[126] Although not specifically focused on TFET devices, their study offers valuable insights into the potential

utility of the RFR approach. The model is trained using labeled data to predict Rc values based on specified inputs, including dielectric constant, trap concentration, temperature, and channel length. The model is notable for its accuracy and efficiency in both classification and regression tasks. The efficacy of RFR in addressing intricate, non-linear relationships between input variables and Rc in OTFTs exemplifies the potential of ML to elucidate and model the complex interdependencies inherent to TFETs. This allows for a better understanding of how different factors affect the overall performance of the device, which, in turn, can inform targeted improvements. The model demonstrated high accuracy rates for a range of parameters that affect Rc, thereby illustrating its ability to provide reliable insights into Rc optimization.

In designing TFETs, this signifies the capacity to anticipate device behavior in response to alterations in material properties, geometries, and environmental conditions. As a result, optimal design configurations for desired operational characteristics can be identified. For example, Akbar *et al.* utilized RFR to predict the performance of TFETs,[127] a methodology that is analogous to that employed by Nirosha *et al.*[126] in their analysis of Rc. Their findings illustrate the efficacy of the model in accurately predicting key TFET metrics, including on-current, off-current, and SS. Other significant findings include the model's ability to identify the most influential factors affecting performance by analyzing various device parameters, which can assist in optimizing the design of TFETs. This approach can significantly enhance the design process by streamlining the development and guiding decisions at early stages. It does so by having the ability to analyze large datasets and identify critical design parameters, as well as providing rapid predictions on device performance, which allows for quicker iterations and optimizations. Furthermore, the employment of ML techniques also contributes to a significant reduction in computational costs.

3. Gradient boosting machines (GBMs) and XGBoost

Extreme gradient boosting (XGBoost) is a specific type of GBMs. It is a supervised classification ML algorithm that has been trained using a Pearson correlation coefficient and an important feature metric in order to evaluate the performance of the training features. Both GBMs and XGB represent a refinement of RFR. They are designed to enhance model accuracy by iteratively addressing prediction errors. These methods employ ensembles of simple decision trees, which enable incremental refinement of predictions.[128] Although they operate in a manner analogous to RFR, GBMs and XGBoost are distinguished by their capacity to train more effectively, which is particularly advantageous when optimizing TFET design parameters. The GBM method is particularly effective in addressing the most challenging data points, thereby facilitating the production of increasingly accurate models. However, if not properly calibrated, GBMs have the potential to overfit, thereby requiring greater computational resources. In addition, they are susceptible to minor alterations in the training dataset, prompting the generation of a new tree.[129] Conversely, RFR provides a robust basis for assessing the significance of parameters. It is user-friendly, requires minimal tuning, and maintains robustness against overfitting while reliably yielding good performance. However, GBMs and XGBoost go further by necessitating fine-tuning. While they may be more susceptible to overfitting if neglected, they compensate by delivering more precise results swiftly. Thus, GBMs and XGBoost are particularly adept at quickly pinpointing crucial design elements that can enhance current efficiency and switching behaviors in TFETs, underscoring their potential to accelerate the design and optimization process in TFET technology.

Chen *et al.* employed the XGB method to examine a multitude of potential heterojunction candidates with the objective of identifying a high-performance 2D vdW metal–semiconductor heterojunction.[130] The ML screening process identified six candidates (BTe–$NbSe_2$, Al_2SO–Zn_3C_2, iAl_2SO–Zn_3C_2, GaSe–NbS_2, GaSe–$NbSe_2$, and GeSe–VS_2) from 1092 candidates that exhibited Ohmic contacts and high tunneling probabilities, which are essential for optimizing contact resistance and enhancing device performance (see Table IV). More importantly, the XGB method is executed in less than 5 s and is demonstrably more efficient than traditional first-principles calculations in terms of both time and cost. This evidence supports the assertion that machine learning is an effective approach for screening materials and that unsupervised assisted algorithms can address the challenge of data scarcity in predicting the behaviors of complex dynamical systems.

Although there has been limited investigation into the use of GBMs and XBG ML methods for TFET device simulation, other

TABLE IV. Minimum interfacial distance (d_{min}), binding energy (E_b), work function of 2D metals (W_m), Schottky barrier height (Φ_{SB}), and tunneling probability (TP) of 27 vdW heterostructures that achieved Ohmic contact. Reproduced with permission from Chen *et al.*, Chem. Mater. **34**, 5571–5583 (2022). Copyright 2022 American Chemical Society.

Systems	d_{min} (Å)	E_b (eV)	W_m (eV)	Φ_{SB} (eV)	TP (%)
BTe–NbS_2	3.88	−0.0179	6.12	−0.0615	2.5960
BTe–VS_2	3.64	0.0857	5.98	−0.2446	3.7205
AlO–VSe_2	3.95	0.0810	5.39	−0.0563	3.1002
AlSe–g	3.96	−0.0360	4.51	−0.3683	3.6162
Al_2SeO–g	3.95	−0.0266	4.51	−0.0200	3.3140
Al_2SeO–NbS_2	3.99	−0.0569	6.12	−0.0031	1.1781
Al_2SeO–VS_2	3.91	−0.0382	5.98	−0.0403	1.1768
GaO–NbS_2	3.90	0.0374	6.12	−0.9749	0.7864
GaO–$NbSe_2$	3.71	0.0925	5.42	−1.1058	1.6569
GaO–TaS_2	3.91	0.0350	5.95	−0.8536	0.6503
GaO–$TaSe_2$	3.98	0.1062	5.41	−1.1026	0.9843
GaO–VS_2	3.99	−0.0201	5.98	−0.9002	0.4457
GaO–VSe_2	3.96	0.0073	5.39	−0.0878	0.6103
GaSe–g	4.27	0.0640	4.51	−0.1232	2.8049
GaSe–NbS_2	3.15	0.0214	6.12	−0.4552	16.5614
GaSe–$NbSe_2$	3.16	0.2820	5.42	−0.3176	31.3775
GaTe–g	3.85	−0.0531	4.51	−0.2456	8.4528
Ga_2SeO–g	3.61	−0.0168	4.51	−0.1289	4.0458
Ga_2SeO–NbS_2	3.71	−0.0370	6.12	−0.0565	1.4988
Ga_2SeO–TaS_2	3.96	−0.0336	5.95	−0.0267	0.9770
Ga_2SeO–VS_2	3.75	0.0214	5.98	−0.2036	1.1305
Ga_2SeO–VSe_2	3.72	−0.0385	5.39	−0.0191	2.5033
Ga_2SSe–g	3.88	−0.0386	4.51	−0.4859	3.0206
InS–g	3.45	−0.0189	4.51	−0.1327	3.4158
InS–NbS_2	3.06	0.1050	6.12	−0.3443	11.4793
GeS–g	4.07	0.0174	4.51	−0.1582	10.3199
GeSe–VS_2	3.38	0.0580	5.98	−0.0050	53.5366

applications of this method indicate that it is a highly useful model for specific applications. In other words, the advantage of employing this methodology for automated design space exploration and parameter optimization, as well as for efficient and accurate performance prediction, is evident. For example, the study by Wang and Ross demonstrated the use of the ML model in predicting travel mode choices.[131] The objective of this study was to determine the relative performance of the XGBoost algorithm in comparison with other models, such as RFR, in the context of transportation data. The XGB model was found to have superior accuracy in predicting travel mode choices, thereby demonstrating its strength in dealing with complex, non-linear relationships with data. The ability to do so is of significant benefit for the exploration of new materials and architectures, as evidenced by the literature. In addition to its accuracy, the model was also able to provide insights into the relative importance of the variables that influence travel mode decisions. This is beneficial when applied to TFET design, as it allows for the prioritization of optimization efforts to enhance device efficiency and effectiveness.

4. Future directions

Given the advancements in TFET technology and the need for precision in device modeling, Pi-NN methods are recommended for further development. Their high-dimensional processing power is already a significant asset, yet their true potential lies in integrating fundamental quantum mechanical principles directly into the neural network framework. This integration is key, capturing the nuances of TFET operation that traditional neural networks may overlook, making Pi-NNs particularly valuable. For exploring the design space, RF is advantageous when dealing with large, complex datasets and when seeking to understand broad trends. RF requires less computational power compared to more complex models and offers easier fine-tuning, although it is less suitable for high-dimensional data. It serves as a solid starting point for initial explorations when the relationships between design parameters and performance are not yet fully comprehended. When the dataset is smaller and the design parameter relationships are intricate, necessitating detailed fine-tuning, GBMs are suggested. GBMs are more resource-intensive but can deliver enhanced performance in such scenarios. They are ideal for optimizing design parameters with subtle impacts on TFET device performance. SVMs are ideal for small- to medium-sized datasets. They are simpler models that might struggle with large volumes of data but can be very effective in well-mapped design spaces with stable, clear-cut relationships. That is, they can define clear boundaries in design optimization challenges and offer clarity when deciding on the best path forward for TFET designs.

ML and MS simulations are set to drive significant advancements in semiconductor device design, offering solutions to limitations in traditional methodologies while introducing novel capabilities. ML interatomic potentials (MLIPs), for example, have emerged as a transformative tool, addressing the computational expense and scale restrictions of DFT.[132] While highly accurate, DFT is constrained by its inability to handle large system sizes and its high computational cost. Meanwhile, MLIPs enable simulations at larger length scales (nm–μm) and longer time scales (ns–μs) with substantially reduced computational costs.[133] However, MLIPs come with their own shortcomings; they lack the ability to model electronic structures, making them unsuitable for critical evaluations of optical, electronic, and photocatalytic properties.[132] For these reasons, DFT remains relevant for specific applications, such as precise exploration of vibrational spectra, as demonstrated by the recent development of the DeepH platform by Li *et al.*,[134] which combines deep learning with density functional perturbation theory to improve efficiency without sacrificing accuracy.

Despite their limitations, ML tools like MLIPs hold significant promise in streamlining device design workflows. They can accelerate high-throughput exploration, optimize parameters, and identify promising candidates with great efficiency. Yet, as highlighted by Liu *et al.*, the accuracy of MLIPs hinges on the quality of their training datasets, which often exhibit discrepancies in modeling defect structures, migration barriers, and atomic dynamics during simulations.[133] Approaches such as rare-event (RE)-based error evaluation provide a pathway for refining ML models without resorting to computationally expensive simulations.

Looking ahead, it is evident that the future of device design lies in a balanced integration of ML, MS simulations, and traditional modeling. ML methods such as deep learning are particularly suited for targeted applications, such as photonic device design, while variational autoencoders and other architectures hold potential for optimizing specific processes.[135] However, traditional modeling methods, with their robust physical underpinnings, remain critical for ensuring accuracy in areas where ML alone cannot yet suffice. Future efforts must focus on tailoring ML tools for specific applications, ensuring that they are used in ways that optimize their unique strengths and offer interpretability. By advancing ML methodologies and improving training datasets, the combination of ML and MS simulations will not only enhance efficiency and scalability but also deepen our understanding of materials and devices. These efforts will accelerate the discovery and optimization of next-generation semiconductor technologies, furthering innovation while maintaining rigor.

VI. CONCLUSION

Through our thorough discussion of the application of various 2D materials for TFET design, it is evident that each material group offers specific advantages depending on the application. While direct bandgap materials are preferred for TFET devices, they may not be suitable for traditional transistors, making it crucial to consider the intended application when selecting materials. BP, with its anisotropic properties, tunable bandgap, and potential for a low SS, is ideal for low-power applications. Group III–V materials are generally well-suited for TFETs, offering high on-current and efficient tunneling, making them ideal for high-speed, low-voltage applications. TMDs, with their excellent electrostatic control and direct bandgap in monolayer form, are best for ultra-thin body TFETs and high-speed switching applications. In addition, MS simulations can identify optimal TFET designs without the cost and time associated with experiments. However, integrating quantum models into MS simulations is computationally intensive. In contrast, ML methods efficiently model high-dimensional spaces, making them particularly effective for exploring novel TFET materials and structures. Within our discussion of the ML methods, we have also summarized the suitability of each ML method for simulating TFET performance. This combination of material selection and advanced simulation

techniques is essential for optimizing TFET performance across various applications.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Chloe Isabella Tsang: Conceptualization (lead); Investigation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead). **Haihui Pu**: Investigation (lead); Visualization (lead); Writing – original draft (supporting); Writing – review & editing (lead). **Junhong Chen**: Conceptualization (supporting); Investigation (supporting); Visualization (supporting); Writing – review & editing (supporting).

DATA AVAILABILITY

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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