THE UNIVERSITY OF CHICAGO

SINTERED CADMIUM TELLURIDE NANOCRYSTAL PHOTOVOLTAICS: IMPROVING CHEMISTRY TO FACILITATE ROLL-TO-ROLL FABRICATION

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Abstract

Recent interest in clean, renewable energy has increased importance on cost-effective and materials efficient deposition methods. Solution-processed solar cells utilizing cadmium telluride nanocrystal inks offer a viable method for reducing cost, increasing materials effectiveness, and decreasing the need for fossil fuels in the near future. Initial work focused on developing a useful platform for testing new chemistries for solubilizing and depositing nanocrystal inks. Layer-by-layer deposition using a combination of spincoating, cadmium chloride treatment, and annealing created a photovoltaic-grade CdTe absorber layer. In conjunction with layer-by-layer deposition, a device architecture of ITO/CdTe/ZnO/Al was utilized to create power conversion efficiencies of over 12% with the help of current/light soaking. Detailed exploration of device geometry, capacitance measurements, and intensity- and temperature-dependent testing determined the ITO/CdTe interface required additional scrutiny. This initial investigation sparked three new avenues of research: create an Ohmic contact to CdTe, remove the cadmium chloride bath treatment, and create a roll-to-roll friendly process. Improved contact between ITO and CdTe was achieved by using a variety of materials already proven to create Ohmic contact to CdTe. While most of these materials were previously employed using standard approaches, solution-processed analogs were explored. The cadmium chloride bath treatment proved inconsistent, wasteful, and difficult to utilize quickly. It was removed by using trichlorocadmate-capped nanocrystals to combine the semiconductor with the required grain growth agent. To establish roll-to-roll friendly process, the deposition method was improved, heating source changed, and cadmium chloride bath step was removed. Spraycoating or doctor-blading the trichlorocadmate-capped nanocrystals followed by annealing with an IR lamp established a process that can deposit CdTe in a high throughput manner.

1. General photovoltaic operation and methods for characterization.

1.1. General information on semiconductors and their use in photovoltaics.

Photovoltaics operate on the premise of absorbing light and translating it into electrical energy, called the photovoltaic effect. Electrical power is defined by the presence of a voltage and a current. Without both elements, no power can be generated. Power is generated by a semiconductor, such as silicon (Si), absorbing light. Semiconductors are defined by the presence of an energy gap between the ground and excited states (band gap). A proper balance of voltage and current generated is controlled by changing the band gap. Therefore, understanding the properties of semiconductors becomes paramount to achieving high efficiency photovoltaics.

1.1.1. Semiconductor band gaps and the formation of a built-in potential.

Band gaps in semiconductors arise by bringing many atoms together into a small space, dictated by the lattice constant. In Si, the 3s and 3p orbitals of neighboring atoms overlap to form bonds. As more Si atoms pack together, the number of overlapping atoms increases, bands begin to form, and a gap between bands opens.[1] The bottom band, akin to the highest occupied molecular orbital (HOMO) in molecules, is called the valence band (E_v). The top band, akin to the lowest unoccupied molecular orbital (LUMO) in molecules, is called the conduction band (E_c). The energy difference between the valence band maximum (VBM) and the conduction band minimum (CBM) is the band gap (E_g). The band structure varies with material and crystal structure. The wave vector (**k**) relates the periodicity and directionality of the underlying lattice to the energy for all bands associated with the material. The location of VBM is the Γ valley. For gallium arsenide (GaAs) and cadmium telluride (CdTe), CBM resides in the same wave vector, referred to as a direct band gap.[2] However, Si has its CBM located in the X valley, resulting in an indirect band gap. Indirect band gaps require a change in electron momentum to absorb photons.[2] The change in momentum comes from a lattice vibration (phonon). The requirement for Si to absorb a photon accompanied by a phonon decreases the probability of photon absorption. The implications of this phenomenon on photovoltaics will be discussed later.

Semiconductors at 0 K have completely filled and empty E_v and E_c, respectively. However, as the temperature increases, electrons (e^-) from E_v can achieve enough energy to overcome the band gap (E_g), leaving an open state (hole, h^+) in E_v. The population of e^- (n_i) in E_c (and h^+ in E_v) follows an Arrhenius equation related to the density of states in E_v (N_v) and E_c (N_c) as well as E_g (Equation 1.1).[3]

$$(1.1) \qquad n_i = \sqrt{N_c N_v}\, e^{-E_g/2kT}$$

where k is Boltzmann's constant and T is the temperature in Kelvin. As the band gap of a material increases, the intrinsic carrier concentration (n_i) decreases exponentially. The product of the two densities of states (N_c and N_v) affects n_i and are related to the effective mass of an electron (m_n*) or hole (m_p*). The effective mass connects N_c and N_v to the curvature of the corresponding bands (Equations 1.2 and 1.3).[3]

$$(1.2) \qquad N_c = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} \text{ or } N_v = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2}$$

$$(1.3) \qquad m_n^* = \frac{\hbar^2}{d^2E_c/d\mathbf{k}^2} \quad \text{or} \quad m_n^* = \frac{\hbar^2}{d^2E_v/d\mathbf{k}^2}$$

where h (ħ is h/2π) is Planck's constant. As the curvature of the bands decreases, the corresponding effective mass and the density of states increases. The effective mass also relates to the mobility (μ), or how easily an electron drifts through a material (Equation 1.4).[3]

$$\mu_n \equiv \frac{q\bar{t}}{m_n^*} \quad \text{or} \quad \mu_p \equiv \frac{q\bar{t}}{m_p^*} \tag{1.4}$$

where q is the charge of an electron and $\bar{t}$ is the mean free time between scattering events of the electron. Mobility and carrier concentration dictates the electrical conductivity of the designed device structure.

While mobility remains fairly constant for a material at a given temperature, carrier concentration can be changed through intentionally adding impurities to the semiconductor (doping). There are two types of dopants: electron donors (n-type) and electron acceptors (p-type). Electron donors are atoms with one (or greater) electron more than the atom it replaces. Phosphorous (P) and As are n-type dopants for Si (Figure 1.1a).[4] Electron acceptors are atoms with one (or fewer) electron less than the atom it replaces. Boron (B) and aluminum (Al) are p-type dopants for Si (Figure 1.1b).[4]

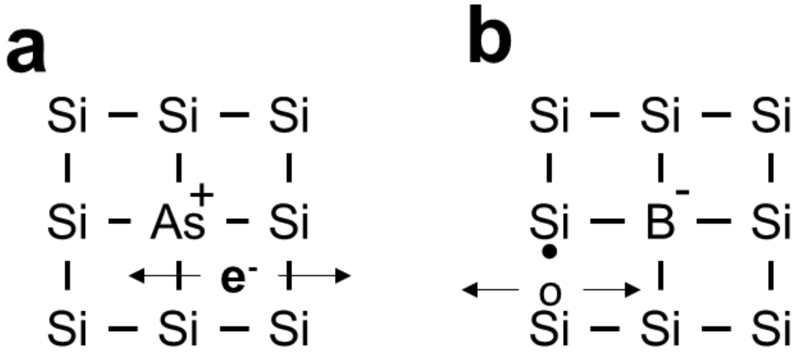

Figure 1.1. (a) N-type doping in silicon by arsenic. (b) P-type doping in silicon by boron.

Accounting for electron deficiency or excess only determines if the impurity atom has the ability to act like a dopant. Another important factor is the energy difference between the donor (or acceptor) state and the conduction (or valence) band (Figure 1.2). For impurities to dope the semiconductor, the difference between energy levels need to be small enough to allow thermalization to take place, like with intrinsic carrier concentrations (Equation 1.1). Otherwise, the impurities will not easily participate in doping and can become trap states.

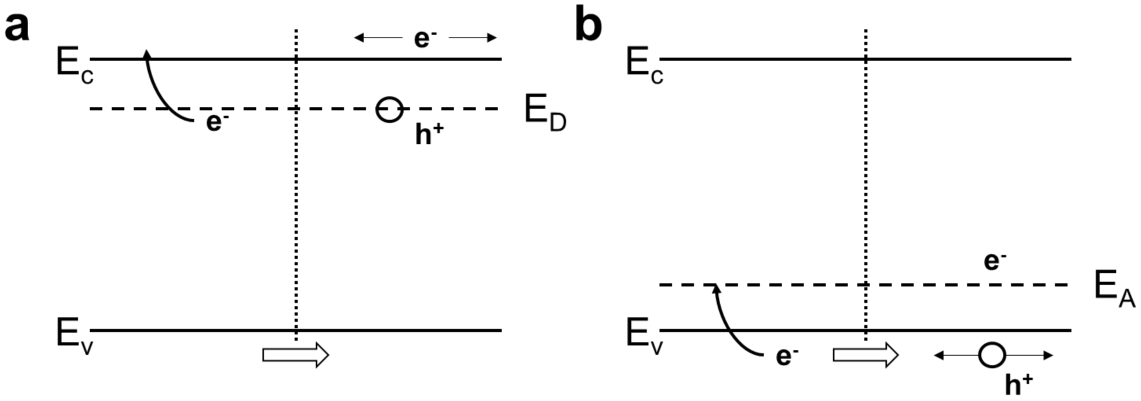

Figure 1.2. (a) N-type doping by emptying of the donor state to the conduction band. (b) P-type doping by filling of the acceptor state from the valence band.

Doping in Si is typically achieved through the use of group III (p-type) and group V (n-type) elements. However, for binary semiconductors, elements from different groups must be used. For III-V semiconductors, group II elements, such as cadmium (Cd) or zinc (Zn), act as p-type dopants while group VI elements, such as sulfur (S) or selenium (Se), act like n-type dopants. Group IV elements, such as Si, is amphoteric, where it can act as n- or p-type, depending on the lattice site it occupies. Transition metals, depending on their ionic species and potentials, can even act as double donors or acceptors. In II-VI semiconductors, doping elements become more complex. Cadmium telluride (CdTe), has a wide array of elements that can dope it. P-type dopants include copper (Cu), silver (Ag), and gold (Au) replacing Cd as well as P and As replacing Te. N-type dopants include indium (In) and Ga replacing Cd as well as chlorine (Cl) and bromine (Br) replacing Te.

As a frame of reference, the intrinsic carrier concentration of Si at room temperature is ~10^{10} cm^{-3} and the lowest impurity concentration achieved has been ~1 part per billion. With atomic density at ~10^{22} cm^{-3}, impurity density is ~10^{13} cm^{-3}. That means base impurity level is 3 orders of magnitude larger than intrinsic carrier concentrations. For materials with a larger band gap (Si is ~1.1 eV), such as GaAs or CdTe, that difference is even larger. Adding elements of the opposite dopant type is one method of overcoming that difference (compensation), but when impurity concentrations are that low, it becomes difficult to control fully.

Carrier concentration is controlled by changing the amount of dopants added to the material. Fermi-Dirac statistics dictate the behavior of electrons in solids (Equation 1.5).

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}} \tag{1.5}$$

where f(E) is the Fermi-Dirac distribution function, E is energy, and E_F is the Fermi energy level. By making the energy level equal to the Fermi level, the exponential becomes e^0, which is 1. The distribution becomes 1/2. Therefore, the Fermi level is defined as the energy where there is a 50/50 chance of being occupied by an electron. By adding dopants, the Fermi is moved up (n-type) or down (p-type) relative to the intrinsic Fermi level. The carrier concentration can be approximated by the concentration of impurities: acceptor concentration (N_A) equates to holes ($N_A \approx p$) and donor concertation (N_D) equates to electrons ($N_D \approx n$). The Fermi level for metals is the work function. In semiconductors, the Fermi level lies in the band gap, making it an imaginary state. It is still a useful measure to explain interactions between layers of different composition. The Fermi level also informs how different electronic components are formed.

Controlling doping allows for the creation of different electronic components used in a wide variety of applications, including microprocessors, memory chips, and photovoltaics (and many more).[5] The most basic electronic component, other than a resistor or capcitor, is the diode. There are two major ways of making a diode: a Schottky contact or a pn junction. A

Schottky contact occurs when a metal contacts a semiconductor and the Fermi levels align to form a barrier potential (Figure 1.3).

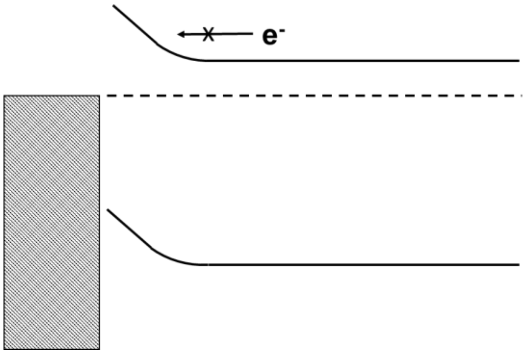

Figure 1.3. Formation of a Schottky contact to n-type semiconductor.

A Schottky contact results in a potential barrier to extracting carriers of a specific type. For n-type semiconductors, electrons are the majority carrier. A barrier to electrons occurs when the conduction band bows upward (seen in Figure 1.3). The valence band bowing downwards is the p-type equivalent. Choosing the metal that contacts the semiconductor becomes increasingly important in all electronics design (and particularly in photovoltaics).

A pn junction occurs when p- and n-type materials are brought in contact with one another. The junction can contain p- and n-type layers of the same material (homojunction) or different materials (heterojunction). Electrons from the n-type layer transfers to the p-type layer and annihilates holes (or fills dangling bonds). The result is two separate charged layers: negative charge in the p-type layer and positive charge in the n-type layer. The charged layer, known as the depletion region, creates a potential difference between the two layers (Figure 1.4).

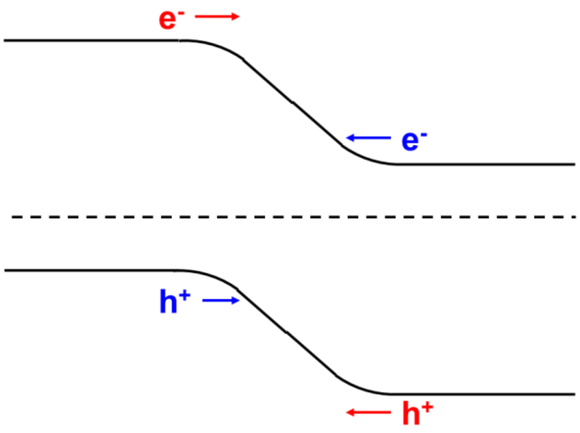

Figure 1.4. Built-in potential formation in a pn homojunction illustrating the occurrence of drift current (red) and diffusion current (blue).

The built-in potential (V_0 or Φ_i) (Equation 1.6) spans the entire depletion region (W) (Equation 1.7) and the two are closely related.[3]

$$V_o = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \tag{1.6}$$

$$W = \left[\frac{2\varepsilon(V_0 - V)}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\right]^{1/2} \tag{1.7}$$

The built-in potential increases as either (or both) of the doping densities increases. The depletion region has a more complex relation to doping densities. It depends both on the built-in potential as well the doping densities of the p- and n-type layers relative to one another. The depletion region also does not have to be evenly distributed between the two layers. Instead, it must be a weighted average between the two. The charge transferred between the two layers must be conserved. The more heavily doped side (p^+ or n^+) transfers a certain amount of charge to the lower doped side. The lower doped side must reach deeper into itself to accommodate it, making the depletion region lie almost entirely in the lower doped side. If the depletion region spans the entire layer, then the diode is referred to as a depleted junction.

Diodes allow current to flow preferentially in one direction. At thermal equilibrium, the current generated from the built-in potential (drift) and the carrier concentration (diffusion) perfectly offset one another for both holes and electrons (as seen in Figure 1.4). The application of an outside potential changes the equilibrium to favor diffusion (forward bias) or drift (reverse bias) currents.

In reverse bias, current is limited by the concentration of carriers. For all voltages, the device follows the diode equation (Equation 1.8) where n=1 is an ideal diode.[3]

$$J = J_0(e^{qV/nkT} - 1) \tag{1.8}$$

where J is the current density, J_0 is the reverse bias current density, and n is the ideality factor (n = 1 to 2). The basic pn junction structure has been applied to a wide variety of materials for use in photovoltaics.

The pn junction becomes a useful method for creating the necessary electromotive force required to separate electrons and holes to generate power during light harvesting. When light is absorbed by the semiconductor, an electron and hole (electron-hole pair, EHP) are generated by exciting an electron from the valence band to the conduction band. EHPs can diffuse within the absorber layer until it reaches the built-in potential. The electron gets swept into the n-type layer while the hole is taken to the p-type layer. The use of a built-in potential to separate EHPs is the basis for photodiodes and photovoltaics.

1.1.2. Solar spectrum and its effect on materials selection.

The generation of a built-in potential creates the electromotive force necessary to produce a photocurrent. Since light absorption depends on the band gap energy and type, materials selection is of the utmost importance. The sun emits light following black body equations (black, Figure 1.5).[6] As light travels through space and reaches Earth's atmosphere (AM0), it is only slightly attenuated (red, Figure 1.5). The atmosphere further attenuates light at specific wavelengths associated with absorption from oxygen and water (blue and green, Figure 1.5) and creates a specific profile at sea level (AM1.5).

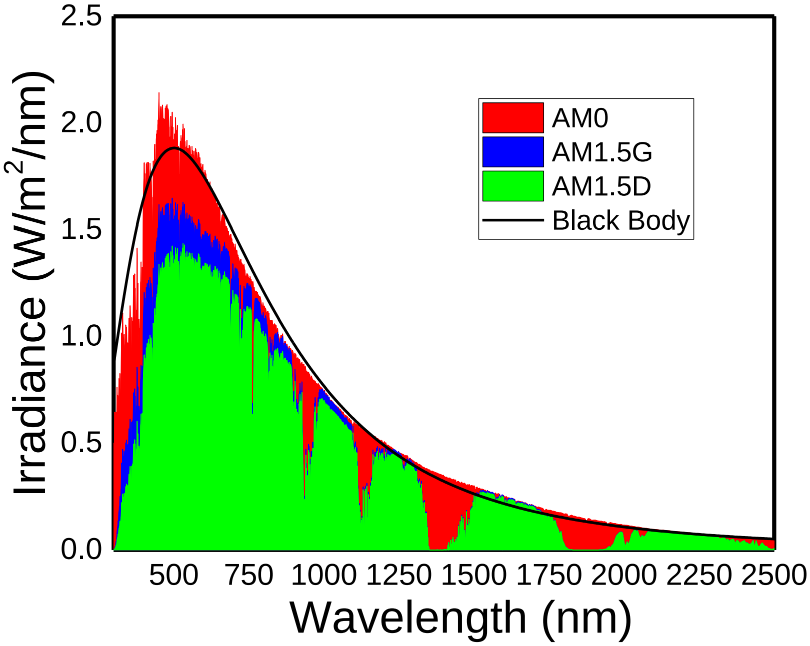

Figure 1.5. Black body radiation profile (black line), solar spectrum at the top of Earth's atmosphere (red, AM0), and solar spectrum at sea level for flat systems (blue, AM1.5G) and solar concentrators (green, AM1.5D).[6-7] Data for the solar spectra were taken from a website by the National Renewable Energy Laboratory (NREL) citing Myers.[7]

Current can be increased by absorbing more light. More photons can be absorbed by increasing the thickness or decreasing the band gap. When the band gap is smaller, it comes at a cost. The maximum achievable voltage is also dictated by the band gap. The energy to excite an electron to the conduction band must by larger than the band gap. However, if the energy of the photon is larger, the excess energy is lost in the form of waste heat. Therefore, the power generated by a solar cell made with a single absorbing material (single junction) has a maximum, referred to as the Shockley-Quisser limit.[8] The Shockley-Queisser limit only takes into account the band gap with respect to the solar spectrum, current generated by EHP collection, and voltage dictated by the band gap. Even in laboratory-scale cells, there are many more considerations, such as series resistance, shunt resistance, and recombination velocities. Taking these factors into account, the maximum efficiency for a single junction solar cell becomes even lower.[9] Even doping and trapping play a role in overall efficiency. Traps in particular cause problems in photovoltaics by contributing to recombination of EHPs before collection.

1.2. Photovoltaics parameters and characterization techniques.

Photovoltaics are tested under normalized conditions by utilizing AM1.5G light. It is defined by the solar spectrum (blue, Figure 1.5) set to a power density of 100 mW/cm^2. Using this as a standard for testing allows for proper comparison between different photovoltaic materials, architectures, and treatments. Typically, light from a source (usually a Xe lamp) is filtered to achieve rough intensities at specific wavelengths and then calibrated to achieve the correct power density. The electronic properties are measured by measuring current under a voltage sweep.

1.2.1. Current-voltage sweeps and extractable parameters.

The current-voltage sweep is the quintessential measurement for evaluating photovoltaic performance. However, only measuring current versus voltage (V) does not yield a proper comparison. The power generated scales by area, so current density (J), typically measured in mA/cm^2, produces a true picture for the efficiency. Graphing so-called JV curves yields useful information on photovoltaic performance (Figure 1.6).

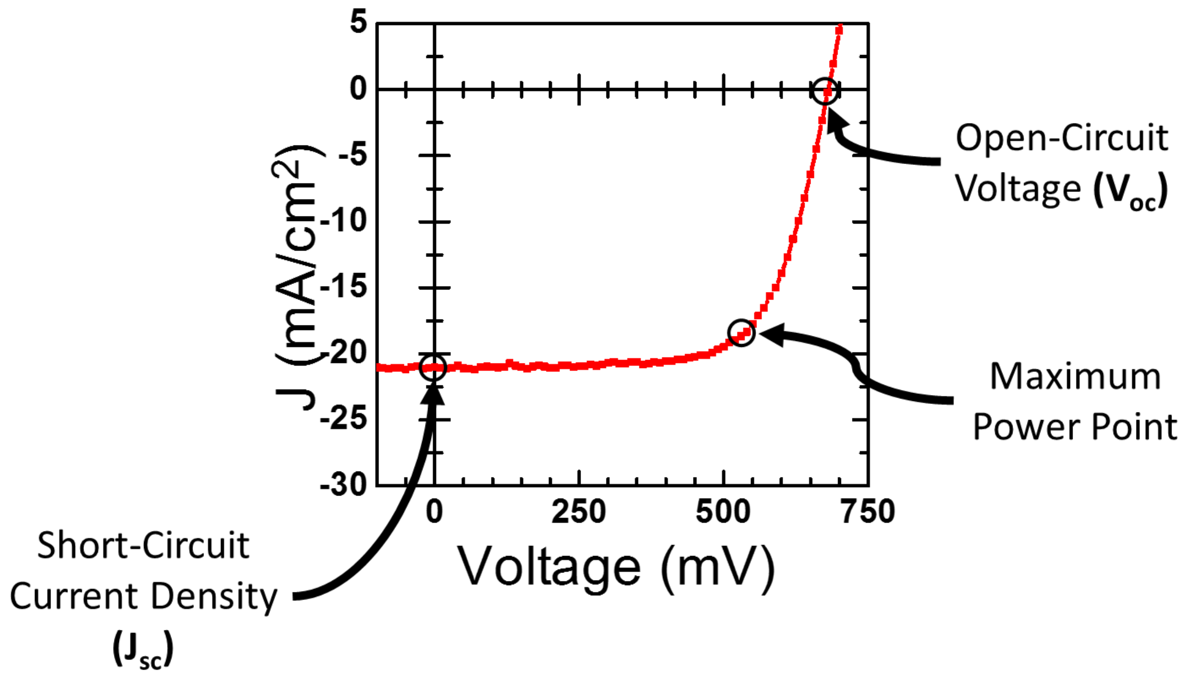

Figure 1.6. JV sweep of a sintered CdTe nanocrystal solar cell using trichlorocadmate-capped CdTe ink. Short-circuit current density, open-circuit voltage, and the maximum power point illustrated to highlight location.

J at zero bias (y-intercept) under illumination is defined as the short-circuit current density (J_{sc}). The voltage with zero current under illumination is defined as the open-circuit voltage (V_{oc}). As previously stated, J_{sc} and V_{oc} limits are dependent upon the band gap and solar spectrum. These values are only part of the power output. Power output requires both a voltage and a current, so the most relevant value is the maximum power (MPP). There are two common methods of finding MPP. The first is to draw a rectangle contained within the axes and the JV curve. MPP is where the area of the rectangle is largest while still remaining within the JV curve. An easier way of conceptualizing MPP is to split power into its two components: current and voltage. Therefore, MPP occurs where the curve created by multiplying the current and voltage reaches a maximum (or a minimum, depending on the formalism). Such an approach makes data processing far easier, especially with the advent of computers. Current density at MPP (J_m) and voltage at MPP (V_m) lead to the maximum power density (P_m) at MPP. P_m is directly converted to power conversion efficiency (PCE or η) by normalizing for integrated illumination power density (P_s). Since AM1.5G is set to 100 mA/cm^2, PCE is simply P_m in mA/cm^2 (Equation 1.9).[6]

$$\eta = \frac{V_m J_m}{P_s} = \frac{P_m}{100 \, {}^{mA}/_{cm^2}} \tag{1.9}$$

PCE serves as the basis to measure all solar cells against one another. The last of the 4 common parameters used to describe photovoltaic performance against one another is fill factor (FF). FF is calculated by finding the percent area covered by the rectangle from MPP and the rectangle covered by J_{sc} and V_{oc} (Equation 1.10).[6]

$$FF = \frac{P_m}{V_{oc} J_{sc}} \tag{1.10}$$

FF is largely dependent on overall layer characteristics grouped into two major components: series resistance and shunt resistance. Series resistance (R_s) describes current losses through resistance throughout the entire system. Shunt resistance (R_{sh}) describes voltage loss through breakdown pathways not associated with the diode. Overall, these two parameters are accounted for by placing a resistor in series (blue, Figure 1.7) and a resistor in parallel (green, Figure 1.7) to the diode (red, Figure 1.7) and current generator (purple, Figure 1.7).

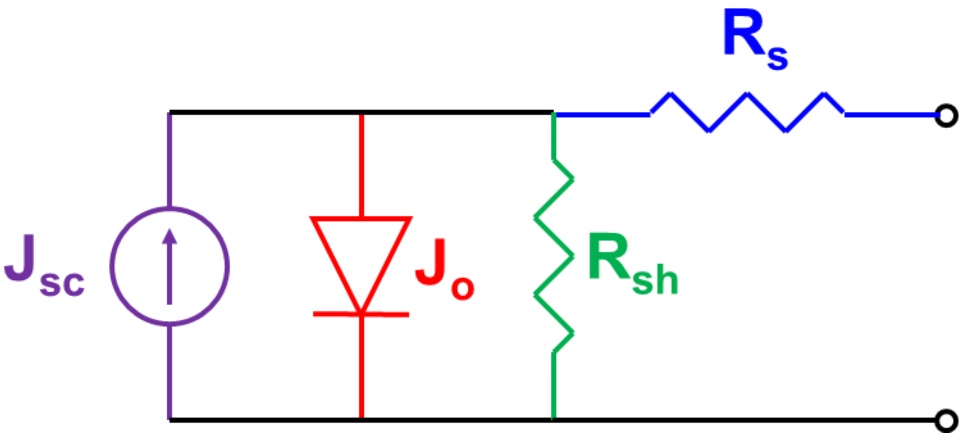

Figure 1.7. Circuitry used to describe series and shunt resistances in photovoltaic operation.

Series resistance is a macroscopic parameter. It helps to describe how easily carriers can travel through the device at larger voltages. An estimation to series resistance is the slope at V_{oc}. It is roughly inversely proportional to that slope. Shunt resistance is a microscopic parameter. It helps to describe how easily charge carriers can travel through the device at smaller voltages. An estimation to shunt resistance is the slope at J_{sc}. It is roughly inversely proportional to that slope. The circuitry described above (Figure 1.7) can be applied with slight adjustments to the diode equation (Equation 1.11).[6]

$$(1.11) \qquad J = J_{sc} - J_0\left(e^{\frac{q(V-JAR_S)}{nkT}} - 1\right) + \frac{V-JAR_S}{R_{sh}}$$

All of these factors affect the overall device performance. They also help to inform certain aspects of the material quality.

1.2.2. External and internal quantum efficiency measurements.

An important measurement for evaluating the device performance, in particular J_{sc}, is external (EQE) and internal quantum efficiency (IQE). EQE is defined as the number carriers collected divided by the number of incident photons. Another way of looking at it is current divided by incident photon power normalized for the charge of an electron and the energy of the photon, respectively (Equation 1.12).

$$(1.12) \qquad \mathrm{EQE}(\lambda) = \frac{J_{sc}(\lambda)/q}{P_S(\lambda)/E(\lambda)}$$

IQE is EQE accounting for the photons reflected (R) back away from the device and transmitted (T) through the device (Equation 1.13).

$$(1.13) \qquad \mathrm{IQE}(\lambda) = \frac{\mathrm{EQE}(\lambda)}{1 - R(\lambda) - T(\lambda)}$$

In most device architectures, the amount of light transmitted is negligible for two reasons: most photons are absorbed and most devices use a metallic back contact. Reflection of light occurs mostly at the interface between air and glass and is calculated through the Fresnel equation (Equation 1.14).

$$R = \left|\frac{n_1 - n_2}{n_1 + n_2}\right|^2 \tag{1.14}$$

where n is the refractive indices for the two layers. Typically, the reflectance for the air-glass interface can be approximated to ~10%. Various anti-reflective coatings have been created to combat this effect and are not the focus of this research.

EQE and IQE help to evaluate current losses throughout the device by observing how different wavelengths interact with the device stack. Shorter wavelength light is more easily absorbed and typically stays within the first 50 nm of the absorbing layer. It is worth noting that glass starts to absorb light with wavelengths shorter than ~350 nm and are not viable for collection under normal circumstances. There are other efforts seeking to emit these photons at lower energies to help harvest this light.[10] Longer wavelengths take more material to absorb and tend to get fully absorbed deeper in the device stack. All of these factors help to give more information on how the device stack performs and potential issues.

1.2.3. Capacitance-voltage measurements.

Capacitance-voltage (Mott-Schottky) measurements are taken to approximate the built-in potential of the device structure. Since the built-in potential helps to separate EHPs, it is important to properly evaluate. Capacitance (C) in the space-charge region (depletion region) can be calculated by oscillating voltage and measuring the response with a potentiostat. Plotting C^{-2} versus V provides a wide variety of information.[11]

There are three major variations from an ideal measurement, all in different regimes. Capacitance will not reach zero if there is voltage sharing between contacts. When there is a rectifying contact along with a p-n junction, then there is the equivalent of two diodes with opposite polarity facing each other. This situation creates a capacitance at the rectifying contact when the entire device is in forward bias because the contact is effectively in reverse bias. The slope of the curve is lower when there are deep trap states. As the Fermi level rises above the level of the of the deep trap states, more states contribute to the capacitance than contribute to doping. Since the doping concentration is inversely proportional to the slope of the curve, the slope decreases with the added states. Finally, a larger voltage can create a state called punch through. Punch through occurs when reverse bias becomes large enough to cause the depletion region to reach the back contact. When this occurs, the capacitance change with respect to voltage ceases. A rough estimate for the built-in potential is achieved by finding the x-intercept. When the measurement strays from ideal, especially in the case of deep trap states, the calculated built-in potential contains large variability.

Harrington et al. goes into a detailed account of how proper measurements can be made without large experimental variability.[12] From the capacitance, the doping concentration of one layer of the device can be calculated (Equation 1.15).

$$\frac{1}{C_{SC}^2} = \frac{-2}{\varepsilon\varepsilon_0 q N_A}\left(V - V_{FB} + \frac{kT}{q}\right) \tag{1.15}$$

where ε is the dielectric constant of the film, ε_0 is the vacuum permittivity, V is the applied voltage, and V_{FB} is the flatband potential. The equation can be simplified by plotting $1/C_{SC}^2$ versus voltage and take the slope (Equation 1.16).

$$\frac{\partial C_{SC}^{-2}}{\partial V} = \frac{-2}{\varepsilon\varepsilon_0 q N_A} \tag{1.16}$$

So long as the difference in doping concentrations between the two layers is at least 3 orders of magnitude, the approximation holds.

1.3. General materials processing concerns.

There are two major applications for photovoltaics: energy for use in space and commercialized energy. Satellites require power to perform basic electronic functions. Solar cells are one of the only technologies properly suited to generate power in space. Satellites need to be as light as possible to leave Earth's atmosphere and travel through space. Therefore, the cell needs to be as efficient as possible to reduce the area needed. In this case, multijunction solar cells made from III-V materials are favored as they produce the highest efficiencies, especially in more intense light (as would be observed in space).[13] Commercial energy needs to be efficient, but it also needs to be inexpensive, easy to produce, and produce more energy through its lifetime than it costs to manufacture. The cost of the module needs to remain low so the consumer remains willing to purchase energy from the company. Multijunction solar cells may be more efficient, but they are also more costly. A company also needs to be able to offset the capital investment used to make the fabrication facility. From this respect, the solar cell must be easy to make so the company can manufacture as many modules in as short of a time as possible. The final, and often overlooked aspect, of renewable energy is the net energy return. If the solar cell requires more energy to manufacture than it produces in its lifetime, then it is not truly a renewable energy source.

Photovoltaics have been made with a wide variety of materials. Si, being an indirect semiconductor, must use more material than its direct gap counterparts. Thin film solar cells made with direct gap semiconductors have increased in relevance, but they still do not compare to Si.

However, with all of the research into improving microprocessors, single crystal silicon has been used as a photovoltaic for decades.[14]

Of the top ten solar energy producing companies, nine of them use silicon in amorphous, polycrystalline, or single crystal forms. The only material to break into the top ten, outside of Si, is CdTe made by First Solar. Currently, the cheapest solar cell in terms of cost per kilowatt hour is CdTe which recently took the lead from polycrystalline Si.[15]

Whether considering Si, CdTe, or even $CuGa_xIn_{1-x}(S,Se)_2$ (CIGS), almost all methods currently employed by commercial solar cells utilize the Czochralksi method or a physical vapor deposition (PVD) method of some sort. PVD's of any sort requires high temperatures, ultrahigh vacuum, or expensive precursors, and sometimes, all three. For instance, the current preferred method for depositing CdTe is close-space sublimation (CSS).[16-17] Typical conditions require high temperatures (~600 °C) and pressures below ~10 Torr. Both contribute to processing costs and tend to decrease high throughput. The hope of solution-processing is to decrease fabrication costs while remaining easy to process and net energy producing.

Solution-processing has many key advantages: does not require high temperatures, can be roll-to-roll friendly, and does not require special atmosphere. All of these factors contribute to decreasing costs. Lower temperatures have added benefits. Most flexible substrates have a ceiling processing temperature of ~300 °C, with fewer having the ability to reach temperatures above 500 °C. Flexible substrates are more roll-to-roll friendly than their rigid counterparts and also make curves possible.

There are many deposition techniques and chemical methods that go into solution-processing. The gold standard for solution-processing is spincoating.[18] The solution is first dispensed onto the substrate which is then spun to create a smooth layer. The overall film properties can be changed by changing the solvent, spin conditions, and many more. The tunability and quality of the resulting film makes spincoating valuable to solution-processing. However, there are a few drawbacks. Large amounts of material is wasted. It does not scale well to large areas. It is a slow process that does not make high throughput easy. All of these factors make spincoating disfavored in roll-to-roll processing. Other methods, such as spraycoating or doctor-blading, have gained favor in industry.

Solution-processing works by dissolving the semiconductor into a solvent. The majority of semiconductors (polymers excluded) require additional chemicals added to the solution to solubilize the semiconductor. For instance, Tiwari et al. made a preparation for CdTe by functionalizing Te and Cd with organic precursors.[19] They can spincoat the resulting compound and react it to form pure CdTe. However, the resulting film has microcracks caused by volume contraction. Since a significant amount of the precursor contains organic components that are removed during processing, volume contraction occurs. Volume contraction creates strain in the film and leads to microcracking in the resulting film. The most effective method of combating volume contraction is through layer-by-layer deposition to fill in the voids. Mitzi found similar success for CIGS and $Cu_2ZnSn(S,Se)_4$ (CZTS) films spincoated with molecular precursors in hydrazine.[20-21]

To combat volume contraction, semiconductor nanocrystals (NCs) have been used to fabricate CdTe,[22] CIGS,[23] and CZTS[24] solar cells. Nanocrystals have the advantage of having about 10,000 semiconductor monomers per building block versus between 100 and 1000. This increases the percentage of semiconductor deposited onto the substrate, minimizing volume contraction in the process. Additionally, NCs already have the semiconductor framework built in, making grain growth a more controlled process.

1.4. Nanocrystal synthesis, ligand exchange, and grain growth.

Since the early 90's, there has been a large body on the controlled growth of semiconductor nanocrystals for use in electronic devices.[25-27] Through precise control over precursor composition and concentration, a wide variety of materials, sizes, and shapes have been synthesized. The sharp control over growth conditions requires the use of long chained organic molecules, which are highly insulating. For many applications, this is not an issue. However, electronic devices require highly conductive materials. Ligand exchanging the surfaces with shorter organic molecules,[28] conductive inorganic molecules,[29] or simply removing surface ligands completely[30] have created many possibilities for controlled functionalities. For some applications, keeping NCs the same is desired. However, for CdTe solar cells, NCs need to sinter into larger grains.[22]

1.4.1. General concepts to II-VI nanocrystal synthesis.

Nanocrystals are typically grown in non-polar solvents using a wide variety of precursors.[25,31] Non-polar solvents must be able to withstand elevated temperatures during hot injection, a common method for NC synthesis. Metal cations are complexed using polar head groups, such as amines, phosphonates, or carboxylates, as surfactant molecules to dissolve the metal precursor in high boiling point, non-polar solvents. Distinct sizes, shapes, and phases of a specific material can be achieved by changing the organic surfactant composition, the metal precursor concentration, and many more parameters. For sintered CdTe NC solar cells, fine control is not necessary because the NCs lose their distinct characteristics during grain growth. A standard metallic precursor for CdTe NCs reacts CdO and oleic acid to form water and an organic salt (Equation 1.17) soluble in non-polar solvents, such as 1-octadecene (ODE).[32]

$$\text{CdO} + 2 \cdot \text{oleate} - \text{H} \rightarrow \text{Cd(oleate)}_2 + \text{H}_2\text{O} \tag{1.17}$$

CdO is basic and reacts with oleic acid at elevated temperatures to form cadmium oleate ($CdOA_2$) and water. Not all metal precursors require an acid-base reaction. Amines form complexes with a metal salt that can be solubilized in the non-polar solvent.

The group VI (chalcogen) precursor has a variety of options as well. Chalcogens react with amines, alkenes, and phosphines to form molecules soluble in non-polar solvents. A typical route for the preparation of soluble tellurium reacts elemental Te and a ternary phosphine (Equation 1.18), such as tributylphospine (TBP).

$$\text{Te} + (\text{C}_4\text{H}_9)_3\text{P}: \rightarrow (\text{C}_4\text{H}_9)_3\text{P}^+ - \text{Te}^- \tag{1.18}$$

TBP and Te react to form as soluble tellurium precursor (TBP-Te). During hot-injection, $CdOA_2$ and TBP-Te react to form CdTe NCs. Growth is controlled through organic ligands binding to the surface. The same ligands used to control growth keep the NCs soluble in non-polar solvents.

1.4.2. Designing functionality to nanocrystals through ligand exchange.

The as-synthesized nanocrystals have long chain organic molecules decorating the surface which prevent effective charge conduction. In the past decade, considerable effort towards functionalizing NC surfaces with conductive, inorganic molecules has yielded a wide array materials. [29,33-34] Typical reactions use a two-phase ligand exchange with long-chain organic-capped NCs dissolved in non-polar solvents layered on top of inorganic ligand solution.

Eventually, the organic ligands are replaced with inorganic ligands, causing the NCs to transfer to the polar phase (Figure 1.8).

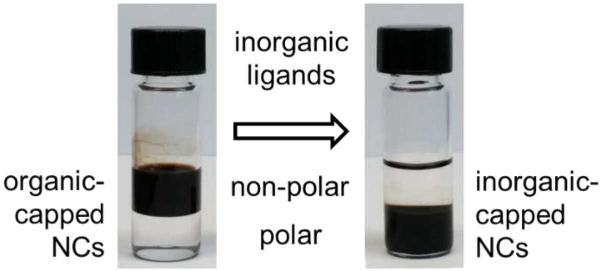

Figure 1.8. Image depicting a typical two-phase ligand exchange going to completion.

Properties like doping,[35] grain growth control,[36] and band structure manipulation[37] become controllable through subtle changes to ligand composition. With such command over materials properties, new and improved technologies can be imagined.

1.4.3. Understanding nanocrystal grain growth.

X-ray diffraction (XRD) and scanning electron microscopy are the two most common methods of monitoring crystallite size evolution in thin film solids. XRD involves bombarding a sample with x-rays and measuring the resulting diffraction pattern dictated by Bragg's law (Equation 1.19).

$$2d\ sin\theta = n\lambda \tag{1.19}$$

where d is the distance between probed planes, θ is the angle of incidence, n is an integer, and λ is the wavelength of the x-ray. Materials have characteristic Bragg angles associated with their phase and lattice spacing. It becomes a useful way to probe a new material to determine distinct chemical species and phases.

Another useful measure is the average crystallite size. The breadth of a specific peak translates to average crystallite size using the Scherrer equation (Equation 1.20).

$$B(2\theta) = \frac{K\,\lambda}{L\cos\theta} \qquad (1.20)$$

where B is the peak breadth at full width-half maximum, K is a shape factor (~0.9), and L is the average crystallite size. The Scherrer equation only gives a rough estimate for size unless a few factors are taken into account: experimental broadening from beam size and shape, detector geometry and distance, and many other factors associated with the measurement. So called Rietveld analysis can produce accurate numbers for grains smaller than ~50 nm.

Nanocrystals start out on the order of ~5 nm in size and they join together into larger grains. The properties of the material can be coltrolled by understanding the grain growth profile with respect to time, temperature, and chemical environment. One method to probe grain growth dependence on temperature (or time) is to prepare samples for each condition. This method is called ex-situ XRD (Figure 1.9).

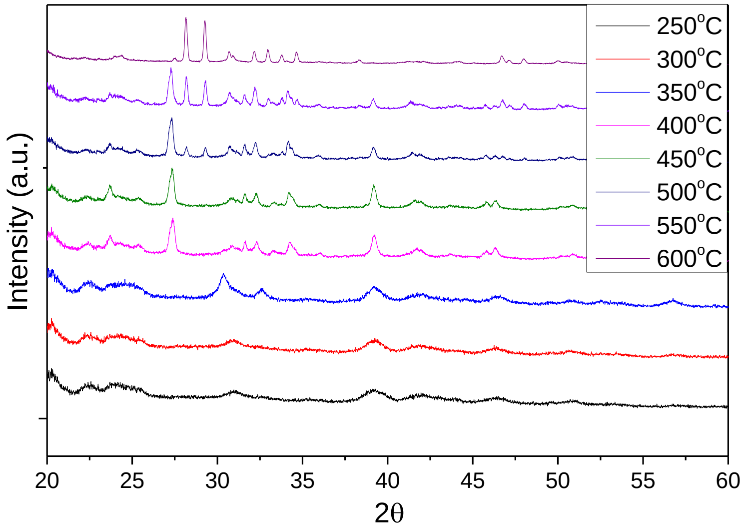

Figure 1.9. Ex-situ XRD of CdTe NCs in the presence of $CdCl_2$ annealed for 3 minutes in air at elevated temperatures.

XRD illustrates the evolution of grain size and chemical species with changes in time and temperature. With the use of a special apparatus to control atmosphere and temperature, it is possible to monitor grain growth over the course of heating (in-situ XRD). This allows distinct monitoring capabilities requiring a limited amount of sample, ~5 mg. A 2D color map can be plotted as temperature versus 2θ with the intensity graphed as a contour map (Figure 1.10).

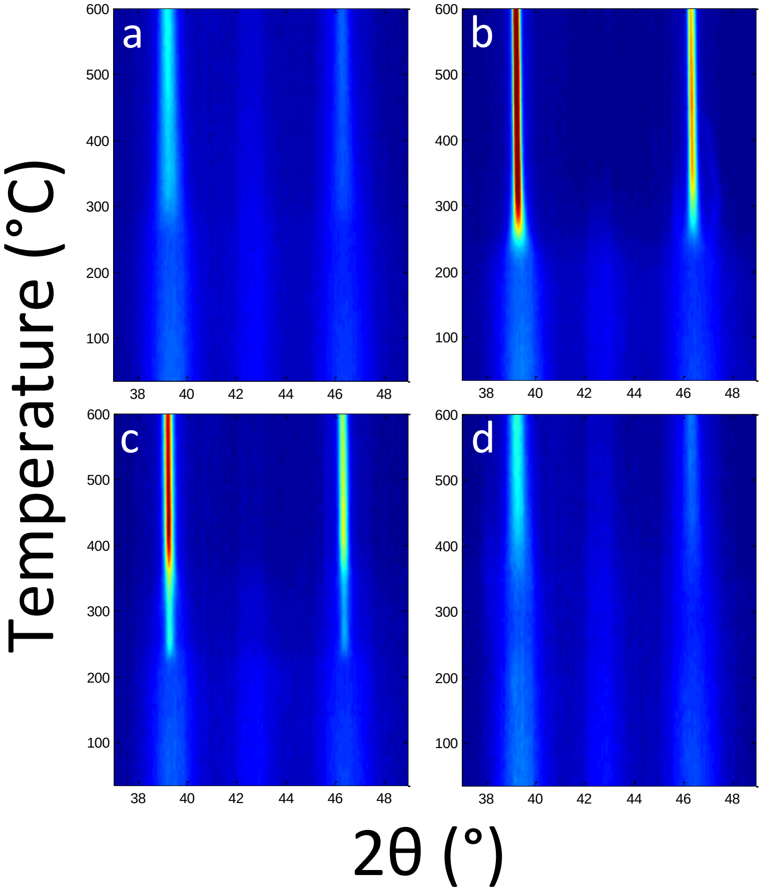

Figure 1.10. 2D color maps of in-situ XRD of CdTe NCs in the presence of pyridine (a), $CdCl_2$ (b), $Cd(ClO_4)_2$ (c), and $Cd(NO_3)_2$ (d). Intensity scales with color where dark red is most intense and dark blue is least intense.

2D color maps are another way of illustrating peak width and intensity evolution with respect to temperature and chemical environment. XRD only gives an average picture instead of fine features.

SEM is an ideal way to understand grain growth and overall morphology. There are two common methods of performing SEM: top view and cross-sectional view. The top view gives a good overall perspective of the film morphology and grain growth (Figure 1.11a). The cross-sectional view gives a better perspective for overall device continuity (Figure 1.11b).

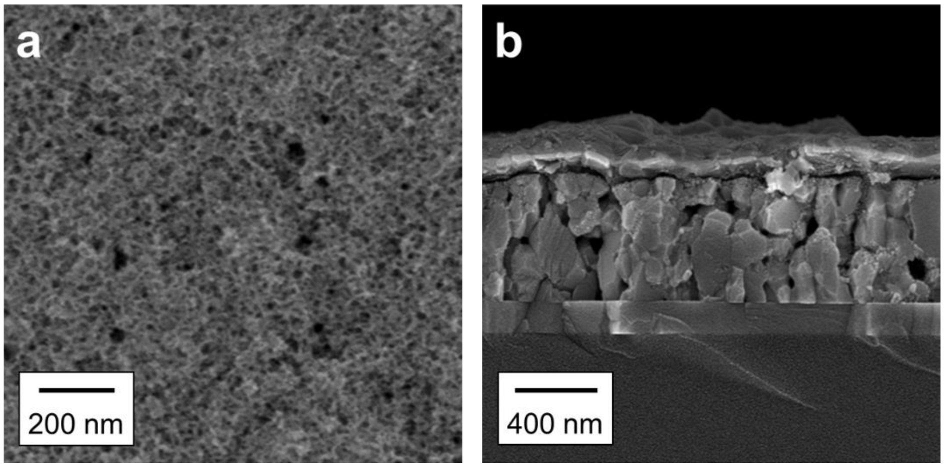

Figure 1.11. (a) Top view SEM of poorly sintered CdTe layer prepared from overwashed $CdCl_3^-$-capped CdTe NCs annealed at 350 °C for 20 seconds. (b) Cross-sectional SEM of CdTe solar cell prepared from $CdCl_3^-$-capped CdTe NCs.

Top view SEM gives complementary microscopic information to macroscopic information from XRD. Cross-sectional SEM gives a glimpse into the device structure from a completed solar cell. All of these techniques are useful in understanding NC chemistry and temperature dynamics necessary for targeting solution-processed semiconductors for use in electronic materials and applications.

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2. High efficiency solution processed sintered cadmium telluride nanocrystal solar cells: the role of interfaces.

Solution processed materials offer a viable alternative to standard deposition methodologies. Dye-sensitized[1-3], quantum dot[4-7], organic, perovskite[8-10] and sintered nanocrystal[11-13] (NC) solar cells are just a few options. In particular, sintering CdTe NCs by performing an in-situ $CdCl_2$ treatment has proven effective at producing a quality absorbing layer. An influential work by Gur et al. first proposed using sintered CdTe NCs as an absorbing layer with PCE of ~ 3%.[14] Jasieniak et al. fabricated a sintered CdTe solar cell with PCE of ~7% by changing the device geometry to indium tin oxide (ITO)-CdTe-ZnO NCs-Al.[15]

2.1. Detailed procedure for standard solar cell fabrication.

The following procedure was created through many iterations to fine-tune the synthesis, ligand exchange, ink formulation, and many other steps involved in the procedure. Prof. Matthew Panthani directed the initial efforts with the help of Travis Dietz. With their initial optimization and probing of the parameter space, I honed the procedure to what it is today. The procedure goes into extreme detail so as to fully explain how to achieve ~11% devices with consistency. To make them 12%, a combination of batch-to-batch refinement and luck is required.

2.1.1. Chemicals used in standard device fabrication.

99.99% trace metal cadmium oxide and cadmium chloride, 90% technical grade oleic acid (OA) and 1-octadecene (ODE), 99.5% by redistillation ethanolamine, 97% tributylphospine with

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isomers (TBP), 99.999% indium chloride, 99.999% tellurium shot and anhydrous hexane, toluene, ethanol, methanol, acetonitrile, pyridine (Pyr), 1-propanol (1-PA) and 2-methoxyethanol were purchased from Sigma-Aldrich. Certified ACS acetone, methanol and 2-propanol (IPA) were purchased from Fisher Scientific. 10 wt% TBP:Te was prepared by dissolving 10 g Te shot in 90 g TBP overnight. ODE and OA were recrystallized by cooling the bottle in a chiller overnight to 12° and 18° C, respectively, and decanted to remove impurities. Pyr and 1-PA were distilled to remove low and high boiling point impurities attributed to morphological issues in spincoated films.

2.1.2. Nanocrystal synthesis and pyridine exchange.

4.80 g CdO, 42.4 g recrystallized OA, and 40.0 g recrystallized ODE were charged in a 500 mL flask and evacuated overnight to remove trace oxygen. The flask was heated to 80° C until the pressure equilibrated. Under dry nitrogen, the mixture was heated to 220° C until the solution turned clear, indicating a completed reaction. The flask was cooled to <90° C and placed under vacuum to remove water generated from the reaction between CdO and OA. The flask was heated to 110° once the solution stopped bubbling and left until the pressure equilibrated. Under dry nitrogen, the flask was heated to 270° C and 24 mL of 10 wt% TBP:Te were injected. The heating mantle was removed immediately and the flask was allowed to air cool to <50° C. The resulting CdTe nanocrystal (NC) solution was split evenly between 8 centrifuge tubes (~16 mL), filled to 20 mL with anhydrous toluene and taken into a dry nitrogen glove box.

The NCs were purified using anhydrous solvents in the glove box. The solution was filled to 37.5 mL with anhydrous ethanol and centrifuged at 4000 rpm for 5 minutes. Following precipitation, the centrifuge tubes were decanted and filled to 20 mL with anhydrous toluene to allow the pellet to dissolve. The solution was washed in this manner 6 times total. Following the third precipitation, the dissolved NCs were centrifuged at 4000 rpm for 1 minute to remove insoluble materials. The soluble NCs were transferred to new tubes. For the last wash, the tubes were filled to 37.5 with ethanol, but no toluene was added after decanting. Instead, 35 mL Pyr was used to dissolve the pellets of 4 tubes using the following procedure:

The solution was stirred at 100° C overnight. Each vial was evenly split into 4 tubes. The NCs were precipitated by filling the tubes to 45 with hexane and centrifuged at 4000 rpm for 20 minutes. The NCs were dissolved in 35 mL pyridine, creating a stock solution.

2.1.3. Dilution test to calibrate the nanocrystal concentration.

The stock solution was tested by pipetting 1 mL from each vial into a centrifuge tube, filled to 20 mL with hexane, and centrifuged at 4000 rpm for 3 minutes. Using solution from each vial makes the overall device fabrication more consistent throughout the lifetime of the stock. The tube was decanted, 2 mL of 1:1 pyridine:1-PA (50/50) was added, and the solution was thoroughly mixed. Three different dilutions were made by taking the solution and diluting to 1 mL with 1:1. 667µL, 571µL, and 500µL of the NC solution was diluted with 333µL, 429µL, and 500µL for 1.5x, 1.75x, and 2x, respectively. The solutions were sonicated for 10 minutes and filtered using a 0.2µm PTFE syringe filter. A layer was deposited by pipetting 325 µL of the NC solution onto a cleaned ITO-coated glass substrate and spun at 800 rpm for 30 seconds and 2000 rpm for 10 seconds. The substrate was dried at 150° C for 2 minutes and air cooled on an Al block. This procedure was followed for each dilution to determine thickness. Figure 2.1 shows typical thicknesses for 1.5, 1.75, and 2x dilution starting with the substrate on the left.

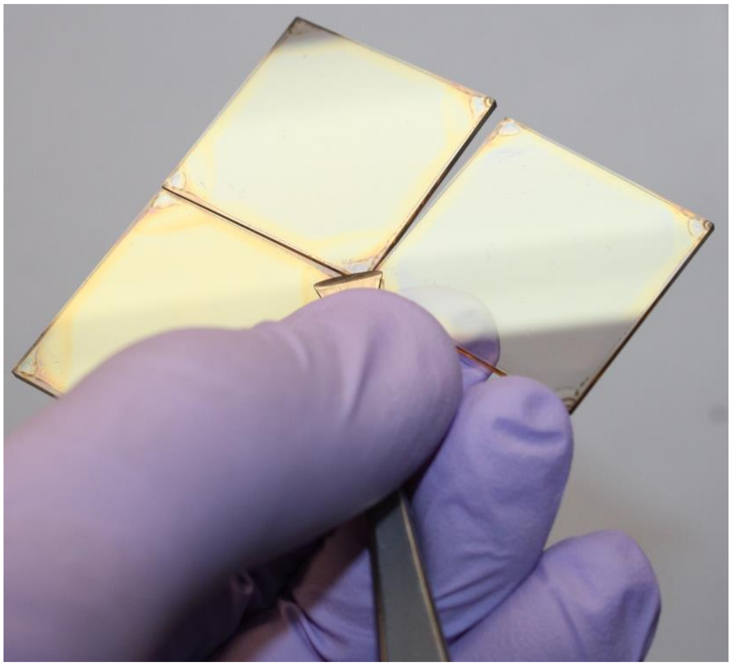


Figure 2.1. Single layer substrates of 1.5 (left), 1.75 (middle), and 2 (right) times dilution. The yellow hue of the leftmost substrate indicates too thick of a layer. The bluish-green hue indicates too thin of a layer. The substrate with a clean green color is an ideal thickness. Usually, the optimal thickness lies within the 1.75x or 2x dilution.

2.1.4. Zinc oxide sol-gel to finish the pn heterojunction.

ZnO sol-gel was prepared by sonicating 1.50 g zinc acetate dihydrate, 15 mL 2-methoxyethanol, 420 μL ethanolamine and 15-45 mg $InCl_3$ together for 1 hour and stirred overnight. Overall, the sol-gel has a shelf life of ~3 months, but is best used before 1 month.

2.1.5. Saturated cadmium chloride bath in methanol.

A saturated $CdCl_2$ in methanol bath was prepared by mixing 1.60 g $CdCl_2$ with 100 mL methanol and heated to 80° C until the powder dissolved. A stir bar can be used to expedite the dissolution process. Typically, it takes about an hour to fully dissolve.

2.1.6. Cadmium telluride nanocrystal ink final preparation.

The amount of stock solution needed depends on how many layers are desired and the results of the dilution test. Typically, 4 substrates can be processed at once. Each layer for all 4 substrates requires ~1 mL of ink plus an extra mL or two to be safe. For a typical stock solution and 16 layer devices, 4.5 mL of stock solution from each vial was pipetted into two centrifuge tubes. The tubes were filled to 45 mL with hexane and centrifuged at 4000 rpm for 3 minutes. The NCs were dissolved using 16 mL of a 50:50 by using 11 mL to dissolve the bulk of the NCs and 5 mL to get the remainder. The solution was transferred to a 20 mL vial, sonicated for 10 minutes and filtered using a 0.2μm PTFE syringe filter.

2.1.7. Standard sintered cadmium telluride nanocrystal solar cell fabrication.

25mm x 25mm ITO-coated glass substrates were purchased from Thin Film Devices Inc. The substrates were sonicated in deionized water (DI) and detergent and thoroughly rinsed with DI. The substrates were then sonicated in DI, acetone, IPA and DI. Following the last DI wash, the substrates were dried using nitrogen and oxygen-plasma treated for 10 minutes using a Harrick PDC-001 Extended Plasma Cleaner. The first layer was deposited by pipetting 325 μL of the NC solution onto the cleaned substrate and spun at 800 rpm for 30 seconds and 2000 rpm for 10 seconds. The substrate was dried at 150° C for 2 minutes and air cooled on an Al block. The substrate was dipped in the $CdCl_2$ bath for 15 seconds, quickly transferred to a beaker containing IPA, thoroughly rinsed with more IPA, and dried under nitrogen flow. The substrate was annealed at 350° C for 20 seconds and quickly transferred to the Al block to cool. The process was repeated until the desired thickness was achieved. The next two layers requires 250 μL ink and the rest only require 225 μL ink because of improved wetting. Following the last layer, 300 μL of ZnO sol-gel was pipetted onto the substrate and was spun at 3000 rpm for 30 seconds. The substrate was annealed at 300° C for 2 minutes and cooled on an Al block (left, Figure 2.2).

Figure 2.2. Image of sintered CdTe nanocrystal solar cells after ZnO sol-gel (left), electrode deposition (middle), and Ag paint contacted to ITO (right).

The substrates were transferred into a glove box and held under high vacuum overnight. The substrates were masked using a homemade substrate holder with 8 mm^2 holes evenly distributed on the interior of the substrate. 100 nm of Al followed by 100 nm of Ag were deposited at ~1 Å/s. The substrates were cooled for ~1 hour (middle, Figure 2.2). Three sides of each substrate were scratched off using a razor blade to expose the ITO. Good electrical contact was established using colloidal Ag paint from Ted Pella Inc (right, Figure 2.2).

2.1.8. Solar cell testing setup and initial testing procedure.

AM1.5G solar spectrum was created by using a Newport model 67005 Xenon lamp and solar filter. The light was calibrated using a Hamamatsu Inc, S1787-04 Si solar cell fitted into a homemade testing apparatus. The substrates were tested using a Keithley 2400 electrometer controlled with homemade Labview software. The substrates were covered with an aperture mask with 6 mm^2 holes evenly distributed to supply a controlled amount of light to each pixel and remove uncertainty in illumination area. Figure 2.3 shows the diagram for assembling the solar tester electronics.

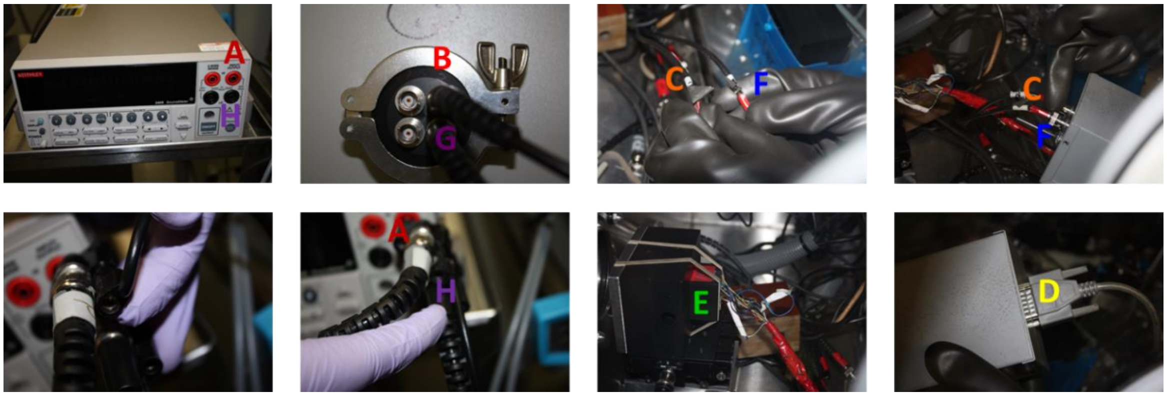


Figure 2.3. Diagram of the solar tester electronics. Starting with the Hi side, the wiring progresses through the alphabet, ending with the letter H, all the way to the Lo side.

Starting at A, a banana plug connector attached to a BNC cable is inserted into the Hi side of a Keithley 2400 electrometer. There are two banana plugs attached to the cable. Choose the Hi side (no bump). The BNC cable then connects to the feedthrough in the back of the glovebox. It inserts in the top right corner, labeled B in the image. This connects to another BNC cable inside the glovebox with the number 2 taped to it, marked C in the image. This BNC cable attaches to the left side of the gray switchbox when the switch is facing towards you and is located on the right side. There is a DSUB connector that plugs into the back of the switch box, marked D in the image. The connector leads to the plugin that works into the back of testing apparatus, marked E in the image. The wiring goes through the device and back out the plugin to the switchbox. The next BNC cable attached to the port in between a BNC port and the switch, marked F, leads out of the glovebox. Another BNC cable, marked G, connects to the feedthrough and leads to another banana plug connector, marked H. H inserts into the Lo side of the Keithley, completing the circuit. The current passes through the central wire of the BNC cable (side with no bump). The outer shielding of the BNC cables are connected using a banana plug to help with noise. While this is most important for low current measurements, it cannot hurt.

The light was calibrated by bumping the legs of the lamp against the guide rail outside the glovebox. The spot was centered on the calibration cell and the focus of the light was adjusted until the current readout of the cell was alternating between 0.75 and 0.76 mA (magnitude). Figure 2.4 shows the correct wiring as well as the correct assembly.

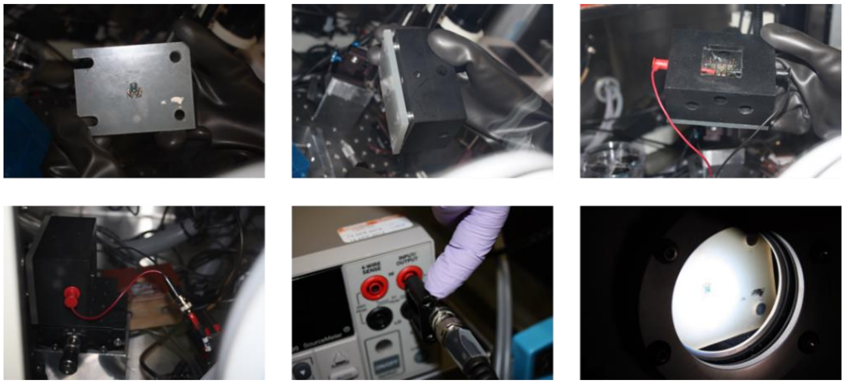


Figure 2.4. Assembly of calibration setup and spot alignment.

A single BNC cable assembly was used to calibrate the light source. The red gripper goes to the left and the black goes to the right. The banana plug matched Hi to Hi and Lo to Lo. To measure the current, the compliance was set to 1 mA and the output was turned on by pressing the grey button marked "ON/OFF". It does not matter which of the BNC cables is used so long as you can measure the current.

With the light calibrated, the device is now assembled into the testing apparatus. The side without the material scratched off and faces down in the testing apparatus. While the actual direction is not important, consistency in the direction is for the current/light soaking procedure. The Al block drops onto the black plastic testing apparatus (BRICK) and is held in place by magnets. There are 13 points of contact to the device: 4 corner connections to ITO and 9 central connections arranged in a square that connects to each individual pixel. The 4 corner connections are all connected together within the switchbox while the pixel connections are separated. The plugin, marked E in Figure 2.2, is inserted into the BRICK and held in place by rubber bands. It is important to keep the rubber bands out of the way of the peg holes (bottom middle) as well as out of the way of the device holes (bottom right). Place the BRICK onto the testing stage by sliding the peg holes over the pegs. This will assure proper alignment.

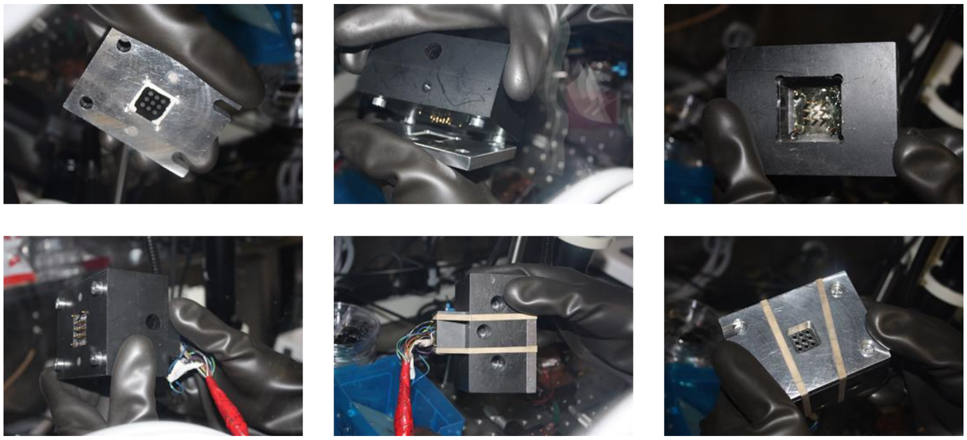
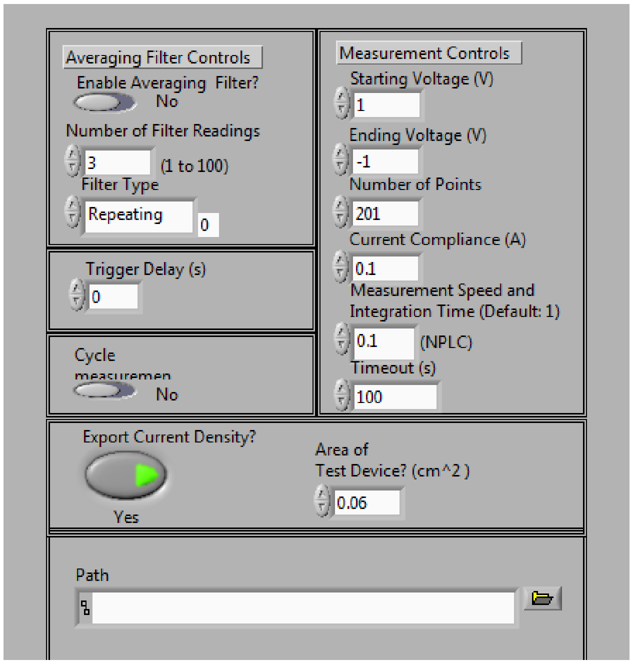


Figure 2.5. Proper assembly for device testing.

With everything setup, log onto the computer with the password. Plug the USB from the Keithley into the laptop. Open the shortcut to the program on the desktop and let it load. Once loaded, input the parameters seen in Figure 2.6.



Averaging Filter Controls
Enable Averaging Filter? No
Number of Filter Readings: 3 (1 to 100)
Filter Type: Repeating 0
Trigger Delay (s): 0
Cycle measuremen No

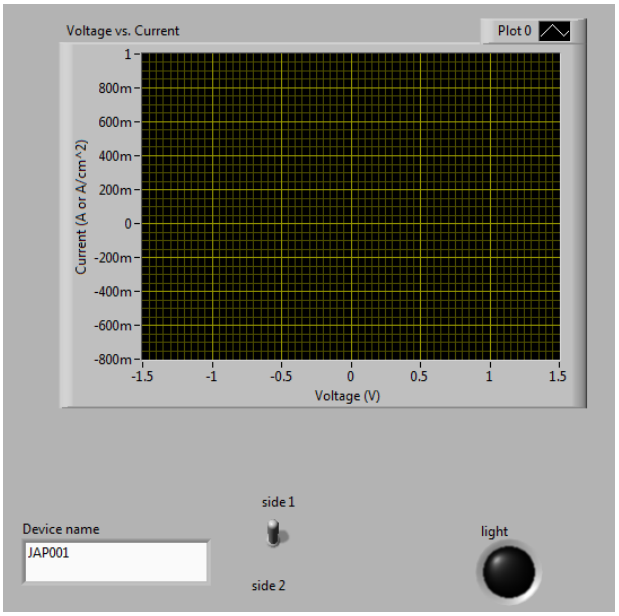
Measurement Controls
Starting Voltage (V): 1
Ending Voltage (V): -1
Number of Points: 201
Current Compliance (A): 0.1
Measurement Speed and Integration Time (Default: 1): 0.1 (NPLC)
Timeout (s): 100

Export Current Density? Yes
Area of Test Device? (cm^2): 0.06

Path

Figure 2.6. Input parameters for IV sweep.

After inputting the parameters, press the folder button seen in the path window. This will open a directory that you need to navigate. Open the folder “Solar Cell” from the desktop. Add a new folder for the date and open that folder. Press “Current Folder” to finish allocating the file pathway. Slide the window over to the testing portion so it looks like Figure 2.7.



Device name
JAP001

Figure 2.7. Testing window.

Type in the device name under “Device name”. Change the selector switch to “side 1” and make sure the “light” indicator is black for testing in the dark and green for testing in the light. To run the program, press CTRL+R.

2.1.9. Standard procedure for current/light Soaking

Following initial testing, 1 pixel from each substrate was chosen for the burn-in procedure. The NPLC was changed from 0.1 to 1.0. The pixel was held at 3 V under illumination for varying amounts of time. Following the current/light soaking, the open-circuit voltage (V_{oc}) was measured by holding the cell under illumination at zero current. When the V_{oc} stabilized, the light and dark IV curves were measured.

The burn-in measurements proceed in the following manner: before Mott-Schottky (MS), after MS, after each burn-in, and after final MS. The burn-in times proceed in the following manner: 15, 30, 45, 60, 90 120, 180, 300, and additional 300 seconds until the V_{oc} stops increasing. To start the burn-in, press the buttons in order seen in Figure 2.8.

Figure 2.8. Button Order to Start Burn-in.

Start by putting the Keithley in local mode by pressing “LOCAL” indicated with 1. This will return the control over the Keithley to the instrument itself instead of the computer. Next, the voltage input needs to change from -1 to 3 V. Start by pressing “EDIT” (2/5), increase the range from 2.1 V maximum to 21 V maximum by pressing “UP RANGE” (3/6), and increase the voltage to 3 V with the “UP EDIT” (4/7). Then, the compliance needs to be increased from 0.105 A to 1.05 A. After 4, quickly press “EDIT” (2/5), increase the compliance with “UP RANGE” (3/6), and increase the compliance with the “UP EDIT” (4/7). Complete everything by pressing “ENTER” (8). It is important to note that if you go too slowly, the edit process will stop and you will start over. Change the value measured by pressing “I MEAS” (9). Open up a timer of some sort so you can accurately gauge how long you do the burn-in and start the process by pressing

"ON/OFF" (10). Remember that burn-in is current/light soaking, so the cardboard box should be up. After the allotted time has expired, the V_{oc} should be measured until it equilibrated. Figure 2.9 shows the button order.

Figure 2.9. Button Order for V_{oc} Equilibration.

Since you are measuring the voltage in open circuit, you need to be sourcing current (0 A) and measuring voltage. Start by pressing "I Source" (1) followed by pressing "V MEAS" (2). Next, the current has to be changed from 10 µA to 0 µA. Start by pressing "EDIT" (3), decrease the current to 0 with "DOWN EDIT" (4), and enter the values with "ENTER" (5). Measure the V_{oc} until it equilibrates and then measure the light and dark IV sweeps. Repeat until the V_{oc} stops increasing, taking light and dark IV sweeps after every iteration.

2.2. Probing the interface between indium tin oxide and cadmium telluride.

The above procedure was utilized from prior knowledge as well as experimenting with different device architectures. Jasieniak et al. utilized the same device architecture with ZnO NCs instead of a sol-gel.[16] Using this as a starting point, other avenues of creating the n-type window layer to contact p-type CdTe were explored.

2.2.1. Changing from zinc oxide nanocrystals to indium-doped sol-gel.

One of the first steps taken to realizing a better window layer for CdTe was to use a different ZnO precursor. CdTe NCs were repeatedly spincoated, chemically, and thermally treated onto ITO-coated glass purchased from Thin Film Devices Inc. in a layer-by-layer fashion to build up the CdTe absorber layer. Originally, ZnO NCs were utilized to make the window layer followed by Al thermally evaporated to complete the device stack (Figure 2.10).

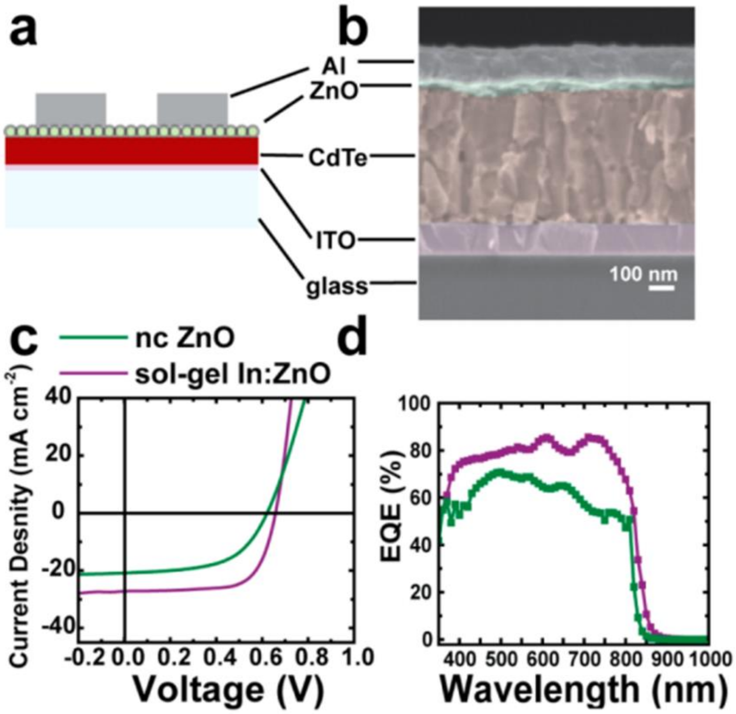


Figure 2.10. Schematic (a) and cross-sectional SEM (b) of a superstrate style device with the following structure: glass/ITO/CdTe/ZnO/Al (false color added for clarity). JV characteristics (c) and external quantum efficiency (d) of devices prepared with colloidal nanocrystal-based ZnO (green) and sol−gel In-doped ZnO (In:ZnO; purple).[17]

By switching from ZnO NCs to an indium-doped ZnO sol-gel, we made a smoother layer with the ability to easily control doping density. Simply changing the ZnO precursor improved series resistance to the point of dramatically improving PCE. The resulting device improved PCE from 7.3% to 12.3%. Most of the improvement came from an increase in J_{sc} (20.8 to 25.8 mA/cm^2) and FF (56 to 71%) with only slight improvement in V_{oc} (621 to 684 mV). However, both devices required current/light soaking to create high efficiencies.

2.2.2. Investigating different device architectures.

To elucidate the cause, a wide variety of device geometries were adopted (Figure 2.11).

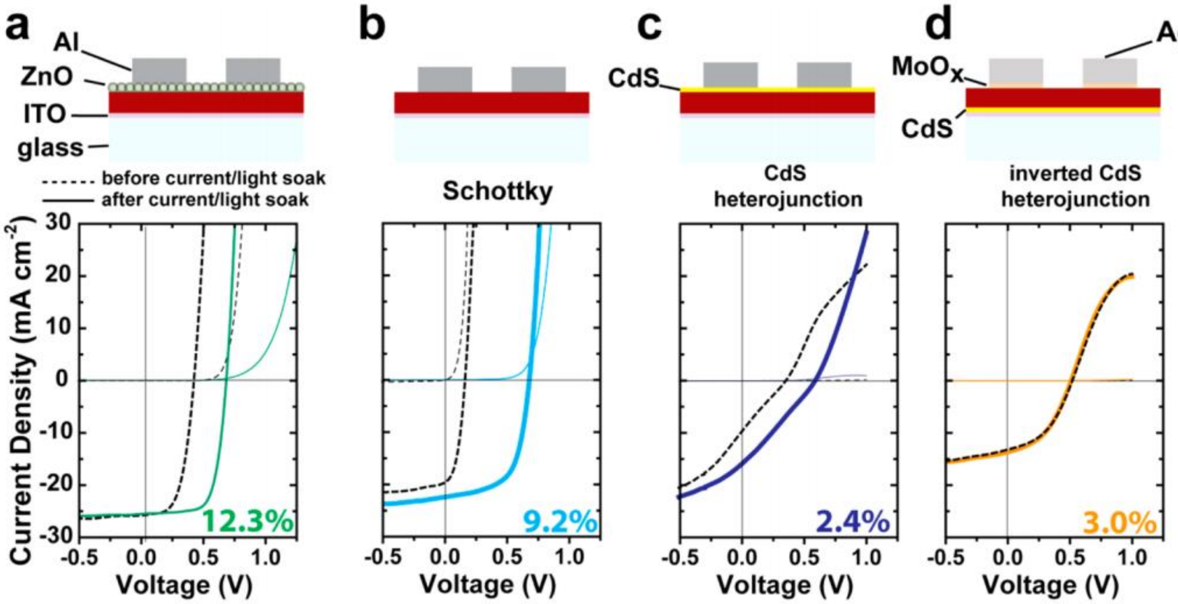


Figure 2.11. Schematics and JV characteristics of different device structures explored in this study. (a) ITO/CdTe/In:ZnO/Al, (b) Schottky structure (ITO/CdTe/Al), (c) CdS heterojunction (ITO/CdTe/CdS/Al), and (d) inverted CdS heterojunction (ITO/CdS/CdTe/Al). JV curves in dashed and solid lines correspond to before and after current/light soaking, respectively. The PCE obtained for each structure is noted.[17]

The Schottky device (Figure 2.11b) not only failed to improve initial device performance but it also had lower PCE upon current/light soaking. Replacing ZnO with CdS (Figure 2.11c) had a similar effect. Once the structure was inverted to remove the CdTe/ITO interface, there was no need for current/light soaking. A device geometry of ITO/CdS/CdTe/MoOx/Ag (Figure 2.11d) had overall lower device efficiency, but V_{oc} (and PCE) remained unchanged from current/light soaking. This device architecture is widely used in high efficiency CdTe solar cell research.

2.2.3. X-ray photoelectron spectroscopy and secondary ion mass spectrometry depth profiling.

The effect current/light soaking has on the ITO/CdTe interface was explored further. Depth profiles using x-ray photoelectron spectroscopy (XPS) and secondary ion mass spectrometry (SIMS) was performed to observe how elemental concentrations are allocated within the film (Figure 2.12).

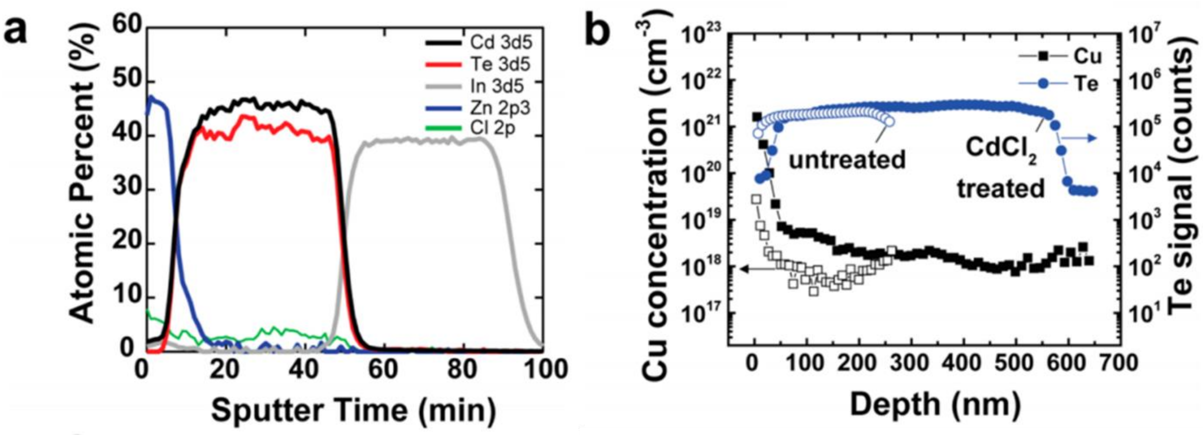


Figure 2.12. Depth profiling using XPS (a) and SIMS (b). The XPS data and $CdCl_2$-treated SIMS samples (panel b, blue and black) were obtained from In:ZnO/CdTe/ITO stacks, while the untreated sample (panel b, open squares/circles) did not have a ZnO layer deposited to rule out In:ZnO film as the Cu source. The SIMS Te counts (circles) are shown as a guide to show the location of the interfaces. Adapted from Panthani et al.[17]

XPS depth profiling reveals sharp interfaces between layers with only slight mixing (Figure 2.12a). Mixing of the ZnO and CdTe layers as well as the CdTe and ITO layers most likely occurs because a combination of annealing and sputtering during the depth profile procedure. Cu, an important dopant in CdTe, was measured using SIMS (Figure 2.12b) to determine the cause of such high concentrations (~2×10^{18} cm^{-3}). SIMS is necessary, versus XPS, because accurate measurements are difficult at such low concentrations. Films were annealed and measured using SIMS with and without $CdCl_2$ to determine the source of Cu. It was determined $CdCl_2$ only contributes negligible amounts. While there was a larger concentration of Cu utilizing $CdCl_2$, it can be accounted for by the increased porosity of the film without the chemical treatment. It was postulated the source of Cu was CdO. Cd is typically extracted from zinc ore,[18] which is largely contaminated with Cu.

2.2.4. Low temperature open-circuit voltage analysis and Mott-Schottky measurements.

Using a specially designed setup (Figure 2.13), low temperature V_{OC} measurements before and after current/light soaking were taken to help to determine which aspects of device performance are affected. Green went into detailed calculations to determine how V_{OC} varies with band gap (Eg), temperature (T), generation rate (G), and recombination rate (R(T)) (Equation 2.1).

$$V_{OC} = \frac{E_g}{q} - \frac{kT}{q} \ln\left(\frac{G}{R(T)}\right) \tag{2.1}$$

As temperature decreases, recombination processes decrease as well. Using Equation 2.1, we see that as T → 0 K, the V_{OC} should approach E_g/q.[19]

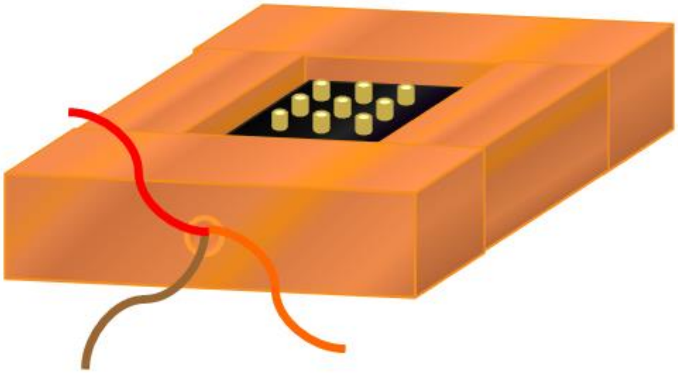


Figure 2.13. Image illustrating the testing setup for low temperature V_{OC} measurements.

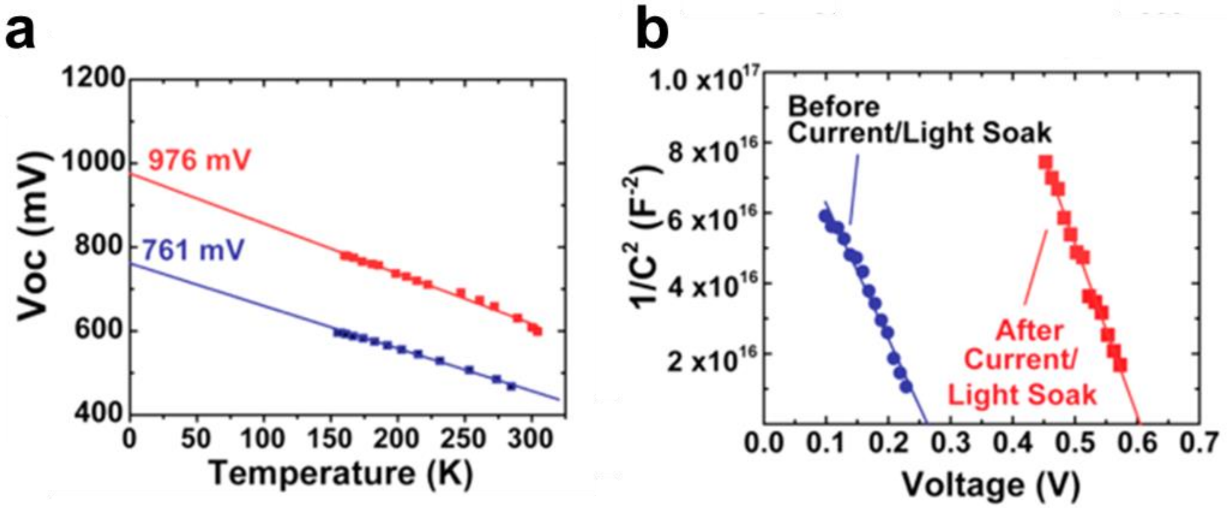


Figure 2.14. (a) Temperature dependence of V_{OC} and (b) Mott−Schottky analysis of a ITO/CdTe/Al solar cell. Both graphs show data before (blue circles) and after (red squares) current/light soaking. The slope of the Mott−Schottky plot gives $N_A = 5 \pm 2 \times 10^{15}$ cm^{-3} before and $6 \pm 1 \times 10^{15}$ cm^{-3} after current/light soaking. Adapted from Panthani et al.[17]

The extrapolation of the V_{OC} (Figure 2.14a) to 0 K falls well below the bandgap of CdTe ($E_g \approx 1.45$ eV) both before and after current/light soaking, indicating that interfaces limit the V_{OC}, rather than Shockley-Read-Hall recombination in the CdTe. Furthermore, the 0 K intercept shifts to a higher potential, but still below Eg, after current/light soaking, indicating that this process reduces an interfacial energetic barrier but does not remove it. We can infer that the V_{OC} is limited by a combination of interfacial effects and SRH recombination within the CdTe and that current/light soaking electronically passivates an interface, increasing the V_{OC}. Upon current/light soaking, the interfacial barrier is reduced and plays less of a role compared to SRH recombination. However, the temperature-dependent V_{OC} data indicates that an interfacial barrier still exists, and addressing this could further improve V_{OC}.

To help determine whether current/light soaking induces any changes in doping within the CdTe layer, we used Mott−Schottky analysis to determine the acceptor concentration (N_A). For this experiment, the Schottky-structure illustrated in Figure 2.11b was used rather than a heterojunction, as this structure has a less complicated equivalent circuit and is more straightforward to analyze. The Mott−Schottky plot shows a clear shift in the built-in potential (x-intercept) from 281 to 629 mV with current/light soaking (Figure 2.14b). The carrier concentration (N_A) calculated from the slope of C^{-2} vs V (Equation 1.16) did not change significantly with current light soaking ($N_A = 5 \pm 2 \times 10^{15}$ cm^{-3} before and $6 \pm 1 \times 10^{15}$ cm^{-3} afterward).

On the basis of the observation that the current/light soak only affects devices that have an ITO/CdTe interface, we can infer that an energetic barrier is being reduced at this interface. This energetic barrier could be a result of poor energetic alignment between ITO and CdTe, perhaps Fermi pinning, which is partially rectified upon current/light soaking. We currently hypothesize that this effect could be related to Cu migration. Similar reversible changes in V_{OC} have been reported during accelerated testing conditions, where devices are held under bias while under illumination and have been attributed to Cu migration.[20] These effects occurred on the time scale of days or weeks (compared to ∼10 min in our case), but are used on much thicker films and may have substantially lower Cu concentrations. The SIMS and XPS data shown in Figure 2.12 indicate that Cu tends to migrate toward the CdTe/ZnO interface, and perhaps the current soaking drives Cu ions toward the CdTe/ITO interface. This suggests that controlling the Cu content within the CdTe could further elucidate the cause of the current/light soaking effect and perhaps provide a pathway toward devices that do not exhibit undesirable transient behavior.

2.2.5. Long term device efficiency measurements.

The steady-state V_{OC} in the CdTe/In:ZnO heterojunction cells decays slowly over the course of several days to weeks to its original value if stored in the dark and more slowly under continuous illumination. We periodically tested a device held under constant AM1.5 illumination over the course of a day (Figure 2.15) after current/light soaking (+3 V, 10 min).

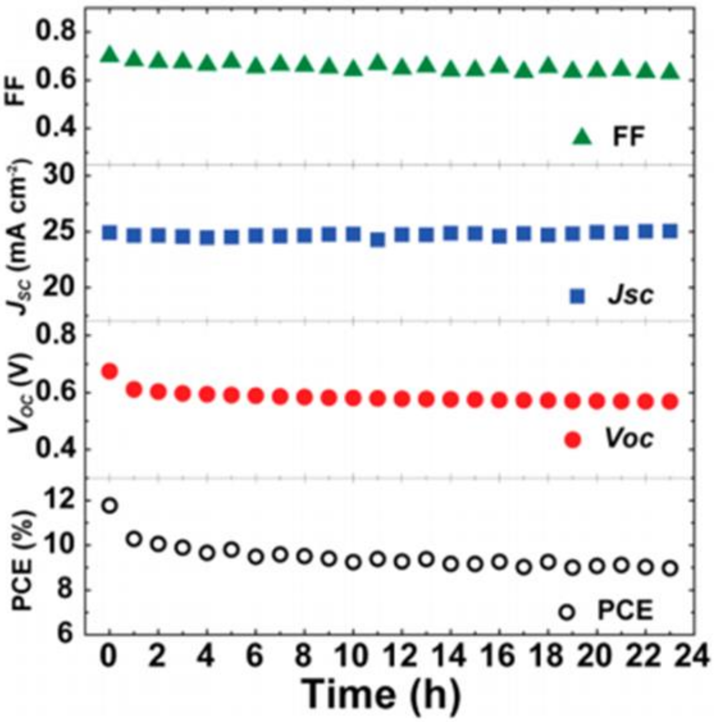


Figure 2.15. Device performance under constant illumination for 24 h measured in air. IV characteristics are taken every 60 min to evaluate the J_{SC}, V_{OC}, FF, and PCE.[17]

The device initially had a PCE of 11.8%, V_{OC} of 675 mV, and J_{SC} of ~25 mA. The V_{OC} dropped by around 10% in the first hour, but only ~15% over 24 h. The drop in V_{OC} was accompanied by a small (less than 10%) decrease in FF. The J_{SC} did not change substantially over 24 h. Subsequent current/light soaking returned the cell's V_{OC} to its high value. After storing a similar device in air for two days and performing a current/light soak, it was submitted to the National Renewable Energy Laboratory's Measurements and Characterization group for testing, showing PCE of 8.54% (Figure 2.16). This lower efficiency can be attributed to decline in V_{OC} over time after current/light soaking, as well as contact oxidation, which reduced the J_{SC} and FF.

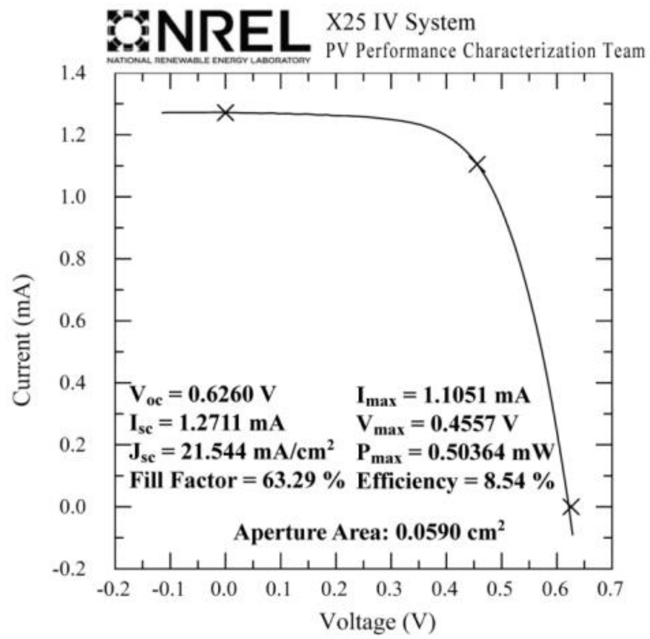


Figure 2.16. IV characteristics taken by the NREL Measurement and Certification group using an X25 solar simulator under standard test configuration. A stainless steel aperture with a 0.059 cm^2 area was placed over the device (active device area ~ 0.08 cm^2). An overall PCE of 8.54% was achieved with a V_{OC} of 626 mV and J_{SC} of 21.54 mA cm^{-2}.[17]

2.3. Continuing with a standardized solar cell fabrication procedure.

This initial work creating new avenues of research. First of all, the ITO/CdTe interface must be improved before further improvements can be made. Second, the $CdCl_2$ bath step proved inconsistent and problematic. Nanocrystal ligand chemistry can easily integrate the semiconductor with the vital grain growth promoter. Finally, spincoating is not a viable option for depositing materials onto large area substrates. Spraycoating and doctor-blading are worthwhile alternatives.

2.4. Acknowledgements.

Prof. Matthew Panthani guided the course of the research and taught me the standard solar cell procedure. I performed many of the experiments on the test setups I designed and built with his input. Dr. Ryan Crisp and Dr. Joseph Luther helped to guide some of the experiments as well as facilitate collaboration with the NREL staff. Travis Dietz and Taha Ezzyat helped to perform

initial experiments and optimization necessary to achieving such high efficiencies. Prof. Dmitri Talapin helped to shape the manuscript so it was worth of Nano Letters.

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3. Transparent Ohmic contacts to a solution-processed cadmium telluride absorber layer for use in photovoltaics.

Recently, solution-processing became a viable route for depositing CdTe for use in photovoltaics. Ultrathin solar cells have been made using colloidal CdTe nanocrystals with efficiencies exceeding 12% PCE demonstrated by using very simple device stacks. The further progress requires an effective method for extracting charge carriers generated during light harvesting. Here, we explored and compared mostly solution-based methods for creating transparent Ohmic contacts to solution-deposited CdTe absorber layer. We demonstrated molecular and nanocrystal approaches to Ohmic hole-extracting contacts at the ITO/CdTe interface utilizing copper-doped CdTe, spincoated Te, and sputtered copper-doped ZnTe that improved PCE without the need for current/light soaking. We used scanning Kelvin probe microscopy to further show how the above approaches improved device collection by reducing the potential drop under reverse bias across the ITO/CdTe interface. Other methods, such as spincoating CdTe/A_2CdTe_2 ($A=Na^+, K^+, Cs^+, N_2H_5^+$) can be used in conjunction with current/light soaking to improve PCE further.

3.1. Establishing Ohmic contact to cadmium telluride photovoltaics.

Given the increasing interest in solar energy, creating high quality absorber layers with efficient electrical contacts becomes increasingly important.[1] CdTe is currently the most impactful thin film photovoltaic (PV) technology, with over 10GW installations. CdTe solar cells provide the lowest cost-per-Watt (~50 cents/W) among current PV technology. Even after 40 years of research, new insights into solar cell improvements, with regards to contacting CdTe, are being discovered.[2-4] Most of the research has focused on physical vapor deposited CdTe, namely close-space sublimation (CSS) and sputtering, the leading technologies for highly efficient CdTe photovoltaics.[5] The majority of solar cells utilize highly doped semiconductors, usually zinc telluride (ZnTe), as a buffer layer for the Ohmic contact to CdTe. Often, copper-doped ZnTe (ZnTe:Cu) has been used as an electron blocking layer at the back contact in the superstrate configuration (light shining through substrate).[4,6-8] Recently, the power conversion efficiency (PCE) of solar cells utilizing the substrate configuration (light shining through top contact) were improved with the aim of using cheaper, flexible metal foils or polymers over more traditional rigid, glass substrates.[9-11] Currently, very few studies have produced a transparent Ohmic contact to CdTe.[12-14] Such contacts are vital for development of tandem PV devices and allow for the creation of transparent photovoltaics to collect excess light from windows. Ultrathin device designs also help to overcome limitations from Te scarcity.

Along with exploring more efficient contacts to CdTe, new methods for solution-processing CdTe have been investigated. Spincoated, sintered CdTe nanocrystals (NCs) were first utilized in solar cells by Gur et al. in 2005 with PCE reaching about 2.9%.[15] Further improvements by Jasieniak et al. increased PCE to around 7% by transitioning the n-type top layer to NC zinc oxide (ZnO) and fine-tuning the deposition parameters of CdTe.[16] Panthani et al.[17] and MacDonald et al.[18] found devices can reach efficiencies of over 10% by using indium-doped ZnO (ZnO:In) deposited via a sol-gel method. In their reports, they determined illuminating the devices under solar simulated light (AM 1.5G) at high forward bias (~3 V) was required to increase device efficiency from ~3-4% to >10% PCE. Such current/light soaking is believed to improve the band alignment at the interface between indium-tin oxide (ITO) and CdTe. While the treatment improves PCE, it does not last, partially decaying over the course of 24 hours and eventually diminishes to slightly better than the efficiency immediately after fabrication.[17]

Few approaches for creating effective electric contacts to CdTe have been explored in conjunction with these new materials processing techniques.[19-20] Fewer studies have determined effective methods for transparent Ohmic contacts to CdTe.[21] In this work, we studied a variety of methods for making transparent contacts to CdTe, including spincoated Te, etched copper-doped CdTe (CdTe:Cu), and sputtered ZnTe:Cu. The open-circuit voltage (V_{oc}) improved dramatically by using these layers between ITO and CdTe, called interfacial layers, with V_{oc}'s reaching almost as high as 700 mV without current/light soaking. Unlike the V_{oc} from current/light soaked devices, the device performance remained for well over a week. We also modeled the device geometry outlined by Panthani et al.[17] and MacDonald et al.[18] to better understand the current/light soaking treatment.

3.2. Cadmium telluride photovoltaic modeling using AMPS-1D software.

Modeled results of the ITO-CdTe-ZnO-Al device stack were generated using AMPS-1D software developed by McElheny et al.[22] Initial parameters tested were chosen from the thesis of Michael David Petersen.[23] There were three major components to the AMPS-1D modeling software: specific layer properties (Table 5.I), electrical contacts (Table 5.II), and light and its absorption (Table 5.III). For optimal fitting, graded "$CdTeO_x$" layers (Table 5.IV) were added to fix reverse bias current and "AlO_x" layers (Table 5.V) were added to achieve rollover and adjust fill factor.

3.2.1. Input parameters for modeled cadmium telluride photovoltaics.

Table 3.I. Relative permittivity, mobility (electron and hole), dopant concentration (acceptor and donor), band gap, density of states (conduction and valence band), electron affinity, thickness, and grid spacing for CdTe and ZnO.[23]

Parameters	CdTe	ZnO
ε_s	9.4	9.0
μ_n (cm^2/Vs)	500	32
μ_p (cm^2/Vs)	60	3
N_A (cm^{-3})	10^{14}	0
N_D (cm^{-3})	0	$1.10\text{x}10^{20}$
E_g (eV)	1.46	3.35
N_C (cm^{-3})	$7.50\text{x}10^{17}$	$2.20\text{x}10^{18}$
N_V (cm^{-3})	$1.80\text{x}10^{18}$	$1.80\text{x}10^{19}$
X_e (eV)	4.26	4.50
t (nm)	550	30
Grid (nm)	5.0	2.0

Table 3.II. Potential barriers, recombination velocity (electrons and holes), and reflection coefficients for current/light soaking progression at the front and back contacts.[23]

	Beginning		Intermediate		Ending	
	Front	Back	Front	Back	Front	Back
Φ (eV)	0.73	0.42	0.90	0.38	1.08	0.36
S_n (cm/s)	10^7	10^7	10^7	10^7	10^7	10^7
S_p (cm/s)	10^7	10^7	10^7	10^7	10^7	10^7
R	0.08	1.00	0.08	1.00	0.08	1.00

Table 3.III. AM1.5G fluence, CdTe absorption coefficient, and ZnO absorption coefficient for given wavelengths.[23]

λ (nm)	Flux ($cm^{-2}s^{-1}$)	CdTe (cm^{-1})	ZnO (cm^{-1})
1000	0.000E+00	1.000E-03	1.000E-03
900	7.310E+15	1.000E+01	1.000E-03
880	7.970E+15	3.000E+01	1.000E-03
860	8.340E+15	2.000E+02	1.000E-03
840	8.020E+15	1.000E+03	1.000E-03
820	7.200E+15	1.340E+04	1.000E-03
800	8.350E+15	1.980E+04	1.000E-03
780	8.600E+15	2.480E+04	1.000E-03
760	8.200E+15	2.920E+04	1.000E-03
740	8.690E+15	3.320E+04	1.000E-03
720	8.050E+15	3.690E+04	1.000E-03
700	8.650E+15	4.050E+04	1.000E-03
680	8.640E+15	4.400E+04	1.000E-03
660	9.360E+15	4.740E+04	1.000E-03
640	9.200E+15	5.080E+04	1.000E-03
620	9.130E+15	5.430E+04	1.000E-03
600	8.710E+15	5.830E+04	1.000E-03
580	8.470E+15	6.300E+04	1.000E-03
560	8.640E+15	6.860E+04	1.000E-03
540	8.490E+15	7.550E+04	1.000E-03
520	8.040E+15	8.420E+04	1.000E-03
500	7.850E+15	9.520E+04	1.000E-03
480	7.710E+15	1.090E+05	1.000E-03
460	7.320E+15	1.270E+05	1.000E-03
440	5.780E+15	1.510E+05	1.000E-03
420	4.860E+15	1.810E+05	1.000E-03
400	3.940E+15	2.210E+05	1.000E-03
380	2.690E+15	2.420E+05	1.000E-03

Table 3.IV. Changes to band gap, layer thickness, and grid spacing for each graded "$CdTeO_x$" layer compared to CdTe.

Parameters	Grade 1	Grade 2	Grade 3	Grade 4	Grade 5	CdTe
E_g (eV)	1.76	1.70	1.64	1.58	1.52	1.46
t (nm)	5.0	5.0	5.0	5.0	5.0	525.0
Grid (nm)	0.5	0.5	0.5	0.5	0.5	5.0

Table 3.V. Changes to donor concentration, band gap, electron affinity, layer thickness, and grid spacing for each graded "AlO_x" layer compared to ZnO.

Parameters	ZnO	Grade 1	Grade 2
ND (cm^{-3})	1.10×10^{20}	0	0
E_g (eV)	3.35	4.20	4.19
X_e (eV)	4.50	3.65	3.66
t (nm)	30	9	5
Grid (nm)	2.0	0.5	0.2

3.2.2. Fine-tuned modeling of the control device.

From the device parameters inputted, the work function of ITO is approximated at ~5.0 eV before current/light soaking (Figure 3.1a). Normally, the work function of ITO ranges from 4.8-5.0 eV based on manufacturer specifications (Thin Film Devices Inc.). The modeled work function lies on the deeper side of the range, which agrees with previous reports.[24-25] Oxygen plasma cleaning, the treatment used to hydrophilize the substrates in preparation of spincoating, was shown to deepen the work function of ITO by removing surface adsorbates. Ding et al. found the work function of ITO was actually even lower, ~5.2 eV.[24] Modeling shows the work function of ITO deepens to ~5.4 eV (Figure 3.1b,d) through the course of current/light soaking, accounting for the change in V_{oc}.

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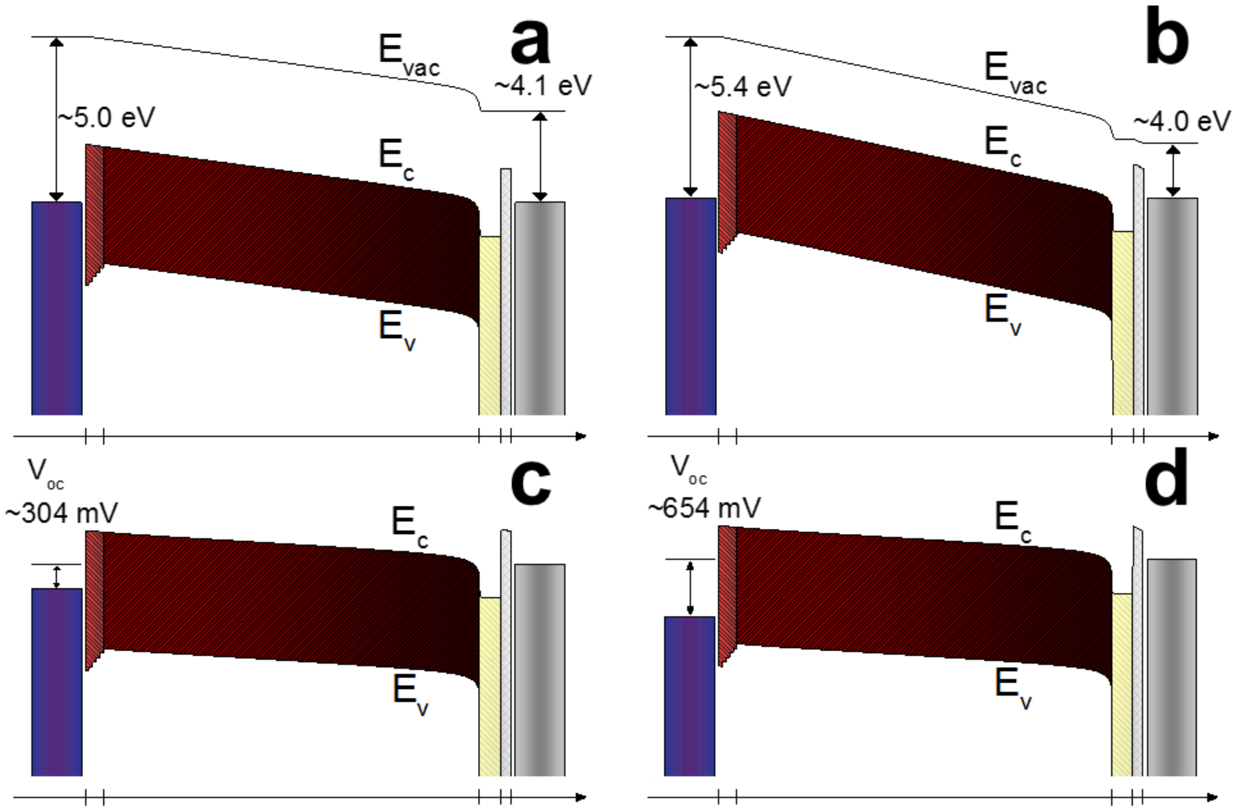

Figure 3.1. Band diagrams of modeled CdTe solar cells with ITO/”CdTeOx”/CdTe/ZnO:In/”AlOx”/Al geometry at equilibrium (a,b) and Voc (c,d) before (a,c) and after (b,d) current/light soaking.

When the work function of ITO is substantially lowered (like after plasma cleaning), it is possible to observe chemical reactions at the interface between ITO and CdTe, resulting in a larger band gap material with a deeper valence band. Oxidation of CdTe can form a variety of compounds ($CdTeO_x$), all of which have a deeper valence band.[26] The addition of this graded layer makes the JV curve more closely match in reverse bias (Figure 3.2).

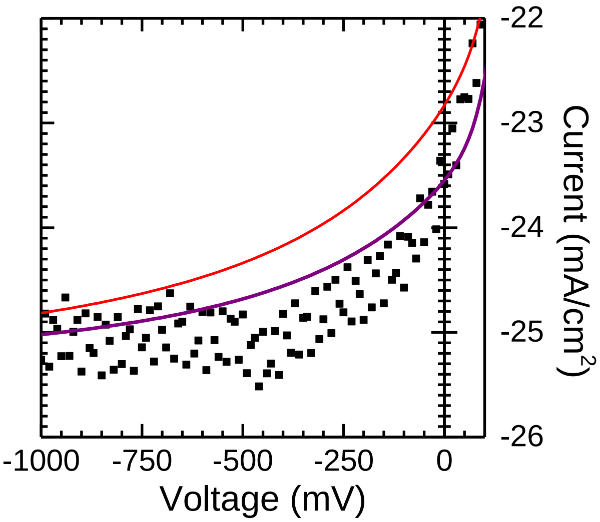

Figure 3.2. Modeled devices with (purple) and without (red) "CdTeO$_x$" layer compared to experimental (squares) JV curves under AM 1.5G. Input parameters for the "CdTeO$_x$" layer can be found in Table 3.IV.

Modeling shows the work function deepens to ~5.4 eV (Figure 3.1b) through the course of current/light soaking, accounting for the change in V$_{oc}$. However, the work function of ITO alone does not account for the overall device characteristics, namely the current plateau (rollover) under forward bias (Figure 3.3) and a decrease in FF.

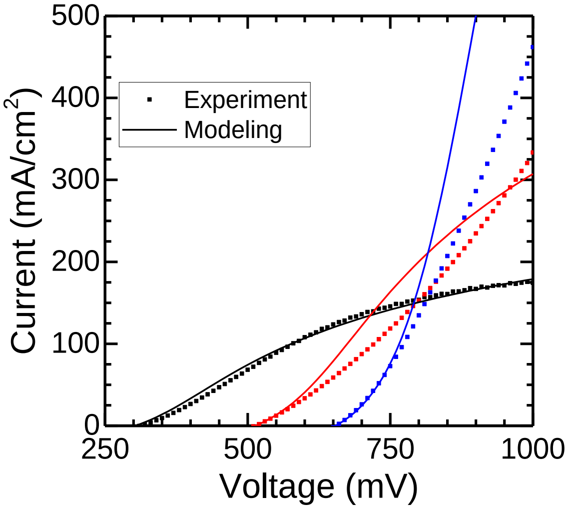

Figure 3.3. Modeled (lines) and experimental (squares) JV curves under AM 1.5G illumination. Input parameters varying the front and back contacts for the beginning (black), intermediate (red), and ending (blue) of the current/light soaking process can be found in Table 3.II.

Modeling showed it is more likely rollover arose from a boundary layer at the IZO/Al interface instead of the ITO/CdTe interface, as previously believed.[27] It is important to note that rollover was not observed in Schottky devices made without IZO.[27] Al has a work function of ~4.1 eV, which lies about 0.4 eV above the conduction band of ZnO.[23,28] Al has the power to partially reduce ZnO to ZnO_{1-x}, oxidizing to aluminum oxide (AlO_x) in the process. AlO_x is highly insulating, which would explain the need to insert a layer between IZO and the back contact. Another explanation can be an electrical barrier between IZO and Al, which is difficult to strictly model.

As the time of current/light soaking increases, more than deepening of the ITO work function occurs. By simply deepening the work function of ITO, rollover remains (Figure 3.4) and FF is lower (Figure 3.5) than it should be, preventing a better match.

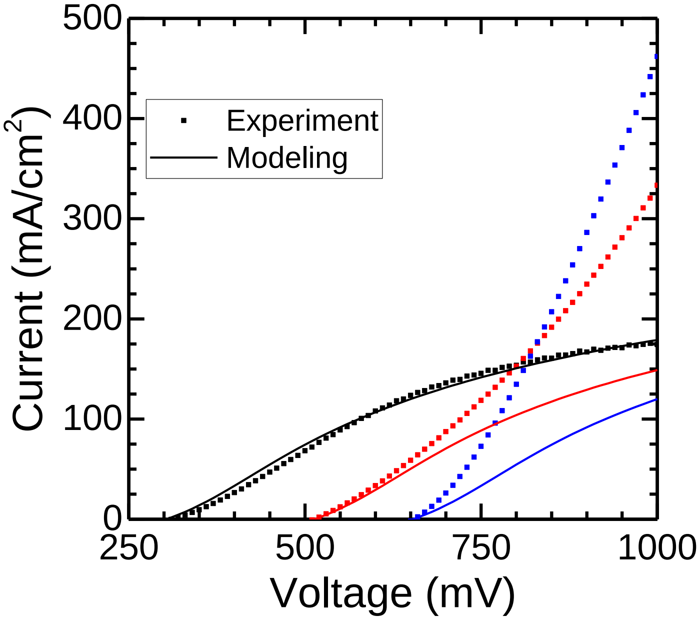

Figure 3.4. Modeled (lines) and experimental (squares) JV curves under AM 1.5G illumination without changing the back contact barrier potentials between the beginning (black), intermediate (red), and ending (blue) current/light soaking cases. The figure focuses on the forward bias regime to illustrate rollover remains unchanged.

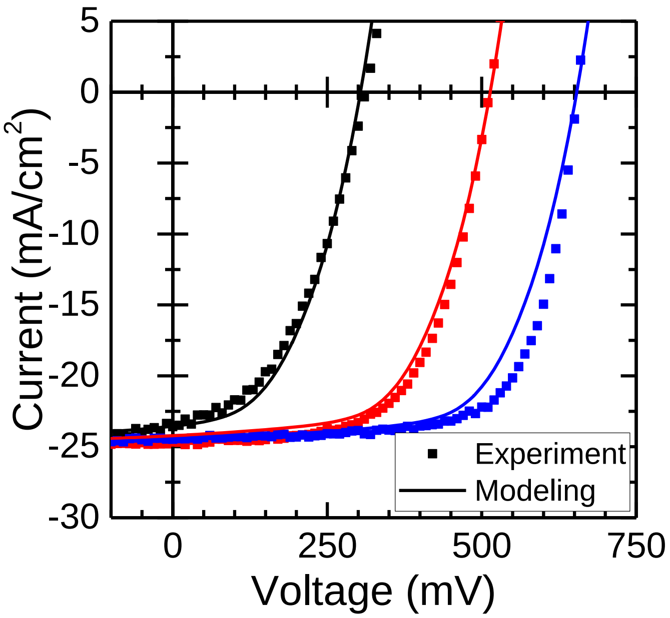

Figure 3.5. Modeled (lines) and experimental (squares) JV curves under AM 1.5G illumination without changing the back contact barrier potentials between the beginning (black), intermediate (red), and ending (blue) current/light soaking cases. The figure focuses on the photovoltaic regime to illustrate the difference in FF between the experimental and the modeled results.

Rollover lessens and FF increases by lowering the barrier potential between AlO_x and the back contact (Al). The initial back contact barrier potential started out at 0.42 eV, making the starting work function of Al ~4.08 eV, matching closely to literature values. To remove rollover and make the FF match more closely, the barrier potential was decreased to 0.36 eV.

Devices current/light soaked for longer time (blue, Figure 3.3) were more difficult to match using modeling. Most likely, this issue could be addressed with the addition of another resistive layer. The sheet resistance of the ITO layer is ~20 Ω/sq, which will add to the series resistance. An increase in series resistance will affect the current in forward bias more significantly, because the effective resistance of diodes is lowered when the turn-on voltage is reached.

An added benefit of a metal back electrode is reflecting transmitted light back to the absorber layer. Using a TCO as an electrode in place of Al would still reflect light according the

Fresnel equation for reflection (Equation 1.14). The refractive index for ZnO:In, ITO, and air are ~2.00, ~1.80, and 1.00, respectively.[29-30] The resulting reflectances for the ZnO:In/ITO and ITO/air interfaces are 0.3% and 8.2%, respectively. Reflectance at the back contact was set to 0.09 to simulate the device curve if a TCO was used instead of Al (Figure 5.6). The lack of a reflective back contact only reduces J_{sc} by ~10%.

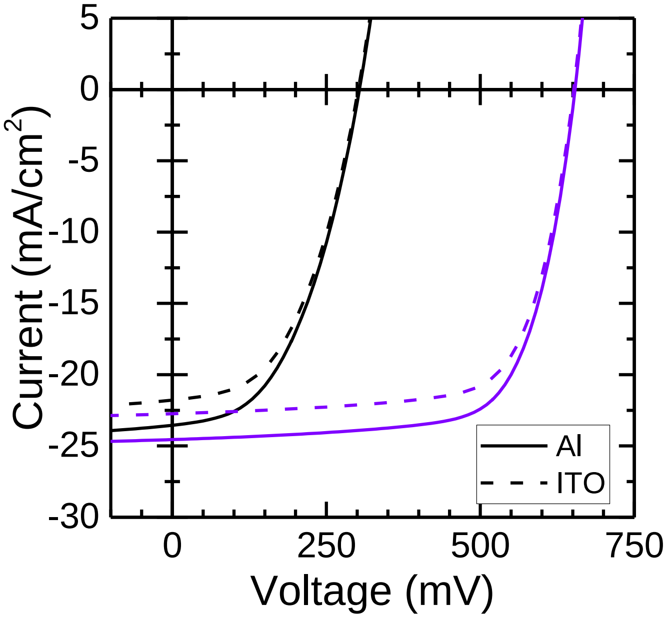

Figure 3.6. Modeled JV curves under AM 1.5G illumination using a reflective (solid) and partially reflective (dash) back contact.

3.3. Experimental route to a stable, transparent Ohmic contact.

3.3.1. Chemicals used to establish transparent Ohmic contacts.

Cadmium oxide (CdO, 99.99+%), tellurium shot (Te, 99.999%), cadmium chloride ($CdCl_2$, 99.99%), zinc acetate dihydrate ($Zn(OAc)_2{\cdot}2H_2O$, 99.999%), indium chloride ($InCl_3$, 99.999%), ammonium iodide (NH_4I, 99.999%), iodine (I_2, 99.999%), copper (II) chloride dihydrate ($Cu(II)Cl_2{\cdot}2H_2O$, 99.999%), silver nanowires (Ag NWs, DxL 120-150nm x 20-50 μm in isopropyl alcohol), copper(II) sulfate ($CuSO_4$, 99.99%), zinc telluride (ZnTe 99.99%), antimony telluride (Sb_2Te_3 99.99%), sodium (Na, lumps in kerosene, 99%), potassium (K, chunks in mineral oil, 98%), cesium (Cs, ingot 99.95%), cadmium telluride (CdTe, 99.99%), Amberlyst 15 hydrogen form (wet), oleic acid (OA, technical grade, 90%), 1-octadecene (ODE, technical grade, 90%), tributylphosphine (TBP, 97% with isomers), toluene (≥99.8%, anhydrous), ethanol (≥99.5%, anhydrous), pyridine (99.8%, anhydrous), hexane (95%, anhydrous), 1-propanol (1-PA, 99.7%, anhydrous), 2-methoxyethanol (99.9%, anhydrous), ethanolamine (99.5%, redistilled), 1-dodecanethiol (DDT, 98%), sulfuric acid solution (1M H_2SO_4), and hydrazine (N_2H_4, anhydrous, ≥98%), were purchased from Aldrich. Acetone (certified ACS), methanol (certified ACS), and 2-propanol (IPA, certified ACS) were purchased from Fisher Scientific. Copper (II) acetylacetonate ($Cu(acac)_2$, 98%) and trioctylphosphine (TOP, 97%) were purchased from Strem. Sodium telluride (Na_2Te, 99.9%) was purchased from Materion. Aluminum (Al, 99.99%) and silver (Ag, 99.99%) pellets were purchased from Kurt J. Lesker Company. PELCO colloidal silver paste (Ag paste) was purchased from Ted Pella, Inc. 10 wt% TBP:Te was prepared by dissolving 10 g of Te shot in 90 g of TBP overnight in a N_2-filled glove box. 1.0M TOP:Te was prepared by dissolving 510 mg Te shot in 4 mL TOP overnight in a N_2-filled glove box. ODE was recrystallized by cooling the bottle in a chiller overnight at 12 °C and decanted to remove impurities. OA was cooled to 16 °C overnight and vacuum filtered to remove high melting point impurities. Pyridine and 1-PA were distilled to remove low and high boiling point impurities. N_2H_4 was purified by distillation and handled in a N_2-filled glove box.

3.3.2. Cadmium telluride nanocrystal ink preparation.

CdTe NCs capped with oleate were synthesized with a modified method described in by Zhang et al.[31] CdO (4.80 g), OA (42.4 g, recrystallized), and ODE (40.0 g, recrystallized) were evacuated in a 500 mL three-necked flask overnight to remove trace oxygen. Afterward, the flask was heated to 80 °C until the pressure equilibrated. Under dry N_2, the mixture was heated to 220 °C until the formation of cadmium oleate as indicated by the solution turning clear. The flask was cooled and dried under vacuum at 110 °C to remove water generated by the reaction. Under dry N_2, the flask was heated to 270 °C, followed by the quick injection of 24 mL of 10 wt% TBP:Te. Immediately after the reaction, the heating mantle was removed and the flask was quickly cooled to room temperature (RT) without additional cooling. The resulting CdTe NCs were purified using anhydrous toluene and ethanol in the glove box.

Following 4-6 purification cycles, CdTe NCs were redispersed in anhydrous pyridine at a concentration of ~80 mg/mL. The solution was stirred under N_2 overnight on a hotplate set to 100 °C, followed by precipitation using hexane. The CdTe NC precipitates were redispersed in fresh pyridine to prepare the CdTe NC stock solution.

3.3.3. Control device fabrication process.

The CdTe absorber layer was spin-coated from pyridine-exchanged CdTe NC ink through a layer-by-layer deposition approach. The following preparation describes the procedure for making a device outlined by Panthani et al. (control device).[27]

In detail, 25 mm×25 mm indium tin oxide (ITO)-coated glass substrates (Thin Film Devices Inc) were cleaned by sequential sonication in deionized water (DI) and Alconox detergent, DI, acetone, IPA, and DI. Afterward, the substrates were dried under N_2, and hydrophilized for 10 min using a Harrick PDC-001 Extended Plasma Cleaner.

The stock CdTe NC solution was precipitated by hexane and dissolved in a 1:1 mixture of pyridine and 1-PA to the desired concentration. The solution was sonicated for 10 min and filtered through a 0.2 μm PTFE syringe filter. The filtered CdTe NC solution was spin-coated onto freshly plasma treated (Section 3a) ITO substrates at 800 rpm for 30 s followed by 2000 rpm for 10 s, dried at 150 °C for 2 min, and cooled in air. For the $CdCl_2$ treatment, the spin-coated CdTe layer was dipped in a saturated $CdCl_2$ bath in methanol at ~60 °C for 15 s, thoroughly rinsed with IPA and dried under N_2 flow. The substrate was annealed at 350 °C for 20 s and cooled in air. The whole process (spin-coating, $CdCl_2$ treatment, thermal treatment) was repeated multiple times (12–20) until the desired thickness was achieved.

The ZnO layer was deposited on top of CdTe by spin-coating 300 μL of ZnO sol-gel at 3000 rpm for 30 s, followed by annealing at 300 °C for 2 min. The ZnO sol-gel was prepared by sonicating a mixture of 1.50 g of $Zn(OAc)_2 \cdot 2H_2O$, 15 mL of 2-methoxyethanol, 420 μL of ethanolamine, and 15–45 mg of $InCl_3$ for 1 h, and subsequently stirred overnight.

The substrates were transferred into a glove box and kept under high vacuum (~10^{-9} Torr) overnight. Top Al contacts (100 nm) were deposited by thermal evaporation through a homemade mask, featured by evenly distributed 8 mm^2 holes. Ag (100 nm) was deposited on top of Al to increase device longevity. Three sides of the device stack were scratched off to expose the ITO. Electrical contact was established using Ag paint.

3.3.4. Interfacial layer chemistry and preparation.

All interfacial layers were deposited onto freshly plasma treated substrates. Following interfacial layer processing, the device was completed using the same procedure as the control devices for proper comparison (Section 3.2.3).

3.3.4a. Iodide/triiodide etched copper-doped cadmium telluride.

A saturated solution of NH_4I in IPA (60 mg/mL) was stirred overnight. To keep the same atomic concentration, a 54 mg/mL solution of I_2 in IPA was stirred overnight. 0.375%

(0.25% or 0.5%) triiodide (I_3^-) with I^- (I^-/I_3^- etch), by at% and not mol%, in IPA was prepared immediately prior to layer preparation by mixing 376 μL (250 μL or 501μL) of 54 mg/mL I_2 in IPA with ~100 mL of 60 mg/mL NH_4I in IPA. A Cu-doped CdTe (CdTe:Cu) layer was prepared by adding 1 part per thousand Cu relative to Cd in the form of dissolved $Cu(II)Cl_2 \cdot H_2O$ to the CdTe NC ink. The solution was spincoated, $CdCl_2$ treated, and annealed following the procedure outlined in Section 3b. Once cool, the substrate was soaked in the I^-/I_3^- etch for varying amounts of time (0, 1, 3, and 5 min). The substrate was thoroughly rinsed in IPA and dried at 150 °C for 2 min.

3.3.4b. Spincoated tellurium from hydrazine.

A stock solution of 1.0M Te in N_2H_4 was prepared by dissolving 1276 mg Te in 10 mL N_2H_4. The vial was stirred until no solid was observed (~1 day). A dark purple solution was achieved. Varying concentrations (0.1, 0.2, 0.3, 0.4, 0.5, and 1.0M) were spincoated at 500 rpm for 6 s followed by 3000 rpm for 30 s. While in the faster stage of spincoating, the solution change from varying shades of purple to a mirrored metallic finish, indicating a chemical breakdown to elemental Te. The substrates were annealed at 200 °C for 30 min in a N_2 glove box and cooled to RT.

3.3.4c. Sputtered copper-doped zinc telluride.

Copper-doped ZnTe (ZnTe:Cu) was sputtered onto cleaned ITO-coated glass with a 2 wt% Cu target. 10, 20, and 40 nm ZnTe:Cu (1, 2, and 4 mins, respectively) was deposited at room temperature with a power of 27 Watts under argon ambient. No further treatments were performed to condition the layer before CdTe absorber layer deposition.

3.3.4d. Spincoated copper(I) telluride nanocrystals.

Cu(I)$_2$Te NCs were synthesized using a method described previously by Kriegel et al.[32] In short, 157 mg of Cu(acac)$_2$ was dissolved in a mixture of 6 mL OA and 3 mL of DDT at 160 °C under nitrogen. Upon stabilization, 200 μL of 1.0M TOP-Te was injected and the flask was held at 160 °C for 30 minutes. The flask was quenched with an ice bath and the solution was transferred air free into a N$_2$-filled glove box. The Cu(I)$_2$Te NCs were purified and ligand exchanged with pyridine using the same procedure outlined in Section 3.2.2. Cu(I)$_2$Te NCs in pyridine were added to the CdTe NC ink at a concentration of 1 part per thousand Cu relative to Cd.

3.3.4e. Spincoated silver nanowires.

Ag nanowires (NWs) purchased from Aldrich were diluted further in methanol and spincoated at 2000 rpm for 30 s. The substrate was dried at 80 °C for 2 min and allowed to cool. This process was repeated once more.

3.3.4f. Electroplated copper.

Cu was electroplated via the method outlined by Pankow.[33] In short, Cu was immersed in a solution of Cu(SO$_4$) and H$_2$SO$_4$. Current and time was varied to deposit a thin layer of Cu, preventing mirroring. The substrate was thoroughly rinsed with DI before deposition of the CdTe absorber layer.

3.3.4g. Spincoated “antimony-doped” zinc telluride from hydrazine.

Antimony-doped ZnTe (ZnTe:Sb) was formed by mixing (N$_2$H$_4$)$_2$ZnTe and Sb$_2$Te$_3$-N$_2$H$_4$ dissolved in N$_2$H$_4$, which were prepared using previously reported methods.[34-35] Briefly, 1 mmol of ZnTe (193 mg) and Te (127.6 mg) were dissolved in N_2H_4. Excess Te was removed from the solution by three successive precipitations and redistributions using N_2H_4/methanol as the solvent/non-solvent combination. The solid resulting from precipitation gradually transitioned from slightly purple to white, indicating removal of excess Te. Sb_2Te_3-N_2H_4 was made by stirring 0.5 mmol of Sb_2Te_3 (313.5 mg) and 1 mmol Te (127.6 mg) in 8 mL of N_2H_4 over the course of two days, resulting in a dark red solution. Sb_2Te_3-N_2H_4 solution was added to $(N_2H_4)_2ZnTe$ solution in varying amounts to form what is believed to be antimony-doped ZnTe ("ZnTe:Sb") solution. The "ZnTe:Sb" solution was spincoated at 800 rpm for 6s and 2000 rpm for 30 s. The substrate was annealed at 350 °C for 30 min.

3.3.4h. Spincoated tellurocadmate-capped cadmium telluride nanocrystals.

CdTe NCs were ligand exchanged using a method described previously.[36] In a nitrogen glove box, 2 mmol A_2Te (where $A = K^+$, Na^+, or Cs^+) was added to 480 mg CdTe powder (2 mmol) in 4 mL N_2H_4. After approximately 2 days of stirring, all solid dissolved and the solution was clear yellow (cloudy green for Cs_2CdTe_2). The solution was filtered with a 0.2 µm PTFE syringe filter, and the solid was isolated by adding acetonitrile as a non-solvent and centrifuging. The solid A_2CdTe_2 was dissolved in N_2H_4 at concentrations of up to ~0.5 M. To create $(N_2H_5)_2CdTe_2$, Amberlyst 15 strongly acidic cation exchange resin was rinsed with N_2H_4 several times to load the resin with $N_2H_5^+$ (4.7 meq/g). The resin was mixed in 10x excess with Na_2CdTe_2 and vortexed briefly. After cation exchange, any excess resin was removed by filtering the solution through a 0.45 µm PTFE syringe filter. Ligand exchange from oleic acid-capped CdTe NCs to A_2CdTe_2 ($A = K^+$, Na^+, Cs^+, or $N_2H_5^+$) was performed in a nitrogen glove box. 10 mL of a solution of oleic acid-capped CdTe nanocrystals in toluene (~8 mg/mL) was layered atop 2 mL of an A_2CdTe_2 solution in N_2H_4 (~15 mM). The solution was briefly vortexed, and the nanocrystals transferred to the N_2H_4 layer. The toluene layer was removed, and the N_2H_4 layer was washed 3 times with 10 mL fresh toluene. Then the nanocrystal solution in N_2H_4 was filtered through a 0.2 µm PTFE syringe filter. This solution was precipitated with the addition of acetonitrile (~1:1 N_2H_4:acetonitrile), and the nanocrystals were redispersed in N_2H_4 (~140 mg/mL). The solution was diluted to ~60 mg/mL and spincoated at 800 rpm for 6s and 2000 rpm for 30 s. The substrate was annealed at 350 °C for 30 min and cooled to RT.

3.3.5. Materials characterization of interfacial layers.

The optical absorption spectra of NC solutions were collected using a Cary 5000 UV-Vis-NIR spectrophotometer in the transmission mode. Scanning electron microscopy (SEM) images of the complete CdTe solar cell devices were acquired on Zeiss-Merlin. X-ray photoelectron spectroscopy (XPS) analysis on I^-/I_3^- etched samples were performed on a Kratos AXIS Nova spectrometer using a monochromatic Al K_α source (hν = 1486.6 eV). The Al anode was powered at 10 kV and 15 mA. Instrument base pressure was 1×10^{-9} Torr. High-resolution spectra in Cd 3d, Te 3d, and Cl 2p regions were collected using an analysis area of 0.3×0.7 mm^2 and 20 eV pass energy.

3.3.6. Device characterization of cadmium telluride photovoltaics.

3.3.6a. Photovoltaic characterization.

Devices were tested under the illumination of a Xe lamp with a AM 1.5G filter (Newport 67005) and calibrated with a Si photodiode with a KG5 filter (Hamamatsu Inc, S1787-04). The illumination area was controlled by a self-aligning stainless steel aperture mask with evenly distributed, nominally 6 mm^2 circular holes (5.94 mm^2 measured). Current density versus voltage (JV) curves were acquired using a Keithley 2400 sourcemeter controlled by a Labview interface. To mitigate heating during measurements, the perimeter of the cell was in direct contact to an Al heat sink. The instruments were controlled and data collected using a homemade Labview program. Current/light soaking was done by applying 2–3 V (forward bias) to the device under illumination for varying amounts of time. Typically, this generated a current density of ~2.5 A cm^{-2}. The current was monitored carefully to not exceed a 3 A cm^{-2}, as current densities greater than this generally caused performance degradation. Holding the devices in reverse bias generally caused a transient decrease in performance (due to reduced V_{OC}). External quantum efficiency (EQE) and interal quantum efficiency (IQE) measurements were taken using Oriel IQE-200 with a step of 20 nm for the wavelength. Capacitance-voltage (Mott-Schottky) data were acquired using a Gamry Reference 600 potentiostat. Data were acquired using a frequency of 500 Hz with an amplitude and step size of 5 and 10 mV, respectively.

3.3.6b. Variable temperature current-voltage curves.

JV curves were taken using the same method described in Section 5a. The substrate was housed in a copper block designed to make electrical contact to the Al/Ag pads, allow light to pass through the glass substrate, and create proper heat transfer so the substrate could be heated or cooled. The device was tested under high vacuum (>10^{-7} Torr) to prevent condensation of water vapor. A Janus Research Co., Inc. ST-500-2-(4TX) cryostage was used to cool or heat the substrate. The temperature was monitored using a Lake Shore Cryotronics Inc. CX-1080-CO-HT thermistor attached to the back of the substrate using heat transfer paste from Omega Engineering. The resistance of the thermistor was monitored with a separate Keithley 2400. AM1.5G light was simulated with a Xe bulb and calibrated by adjusting the photocurrent measured on the device being tested. The saturation current was found by applying homemade Matlab scripts.

3.3.6c. Scanning Kelvin probe microscopy.

Scanning Kelvin probe microscopy (SKPM) can be used to spatially resolve, electrostatic potential profiles of cross-sectioned solar cells (refs). This information can be used to elucidate the relative importance of potential gradients that drive carrier transport and collection, (*e.g.* drift) and concentration gradients (*e.g.* diffusion). SKPM is an advanced electrical variant of Atomic Force Microscopy (AFM), which is based on the measurement of the contact potential difference (CPD) between a conducting coated AFM tip and the sample surface. This CPD is a result of differences in work function (need refs). When the CPD exerts an electrostatic force on the AFM tip, the SKPM feedback loop nullifies this force by applying a DC bias to the tip and thereby recording local work-function variations of the surface. In this section, we describe SKPM mapping of active CdTe solar cell cross sections to characterize potential drops within the device stack as a function of applied bias in order to elucidate the influence of varying interfacial layers.

3.4. The interface between indium tin oxide and cadmium telluride.

As-made devices created by Panthani et al.[17] and MacDonald et al.[18] required current/light soaking that partially degraded over the course of one week. This limitation to device performance was believed to be caused by the ITO/CdTe interface (Figure 3.7).

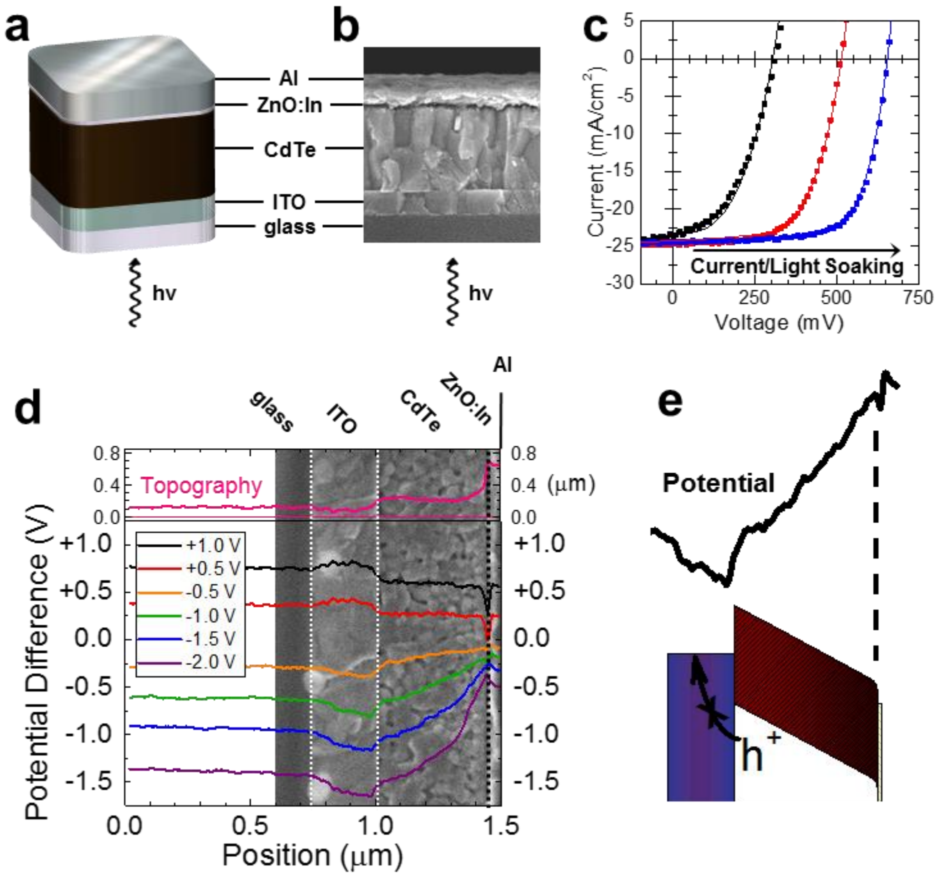

Figure 3.7. Schematic (a) and cross-sectional SEM (b) of control device stack with ITO/CdTe/ZnO:In/Al geometry. (c) JV curves of experimental (squares) and modeled (lines) devices under AM1.5G illumination progressively current/light soaked. Input parameters for modeled JV curves can be found in Supporting Information. (d) SKPM data showing the topography (pink) with the normalized potential difference at +1 V (black), +0.5 V (red), -0.5 V (orange), -1.0 V (green), -1.5 V (blue), and -2.0 V (purple) bias across the device. (e) Schematic and SKPM of potential difference depicting the origin of the potential difference spike under reverse bias (-1 V).

An as-made control device (Figure 3.7a,b) was investigated using cross-sectional scanning Kelvin probe microscopy (SKPM) to spatially resolve the electrostatic potential distribution across the device stack (Figure 3.7d). It showed a pronounced potential difference drop under reverse bias at the ITO/CdTe interface (Figure 3.7e). This spike occurs because of poor contact between ITO and CdTe. Interestingly, the electric field is steady throughout the majority of the CdTe absorber layer, indicating a steady depletion region (green, Figure 3.8).

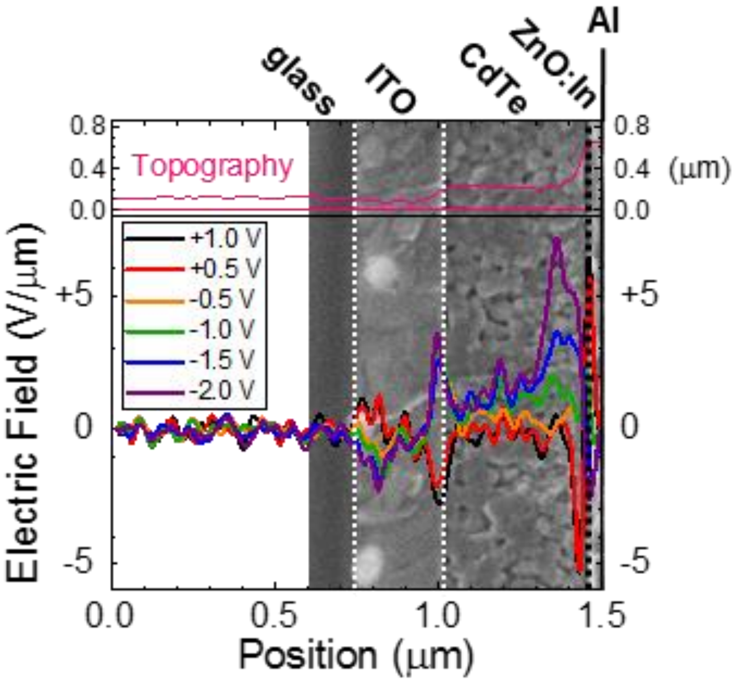

Figure 3.8. SKPM data showing the topography (pink) with the normalized scans at +1 V (black), +0.5 V (red), -0.5 V (orange), -1.0 V (green), -1.5 V (blue), and -2.0 V (purple) bias across the device. SKPM data of normalized electric field overlaid with cross-sectional SEM for the control device without current/light soaking.

Modeling, using AMPS-1D,[22] closely agrees with the JV curves achieved through experiment (Figure 3.7c). It is important to note the inability of the model to account for inhomogeneity of the layers. However, general trends in the device stack can be elucidated. A systematic approach of matching the modeled device curve to the experimental results is outlined in the Supporting Information. As previously believed, the device performance improves as the work function of ITO (front contact) deepens. The short-circuit current density (J_{sc}) improves slightly while the fill factor (FF), V_{oc}, and PCE all increase dramatically. J_{sc} increases because the field strength throughout the device becomes strong enough to extract more of the electron-hole pairs generated from the absorption of photons without an increase in reverse bias. The difference between the V_{oc} before (black, Figure 3.7c) and after (blue, Figure 3.7c) current/light soaking,

~340 mV, can be accounted for by the change in the front contact potential barrier, ~350 meV (Figure 3.9).

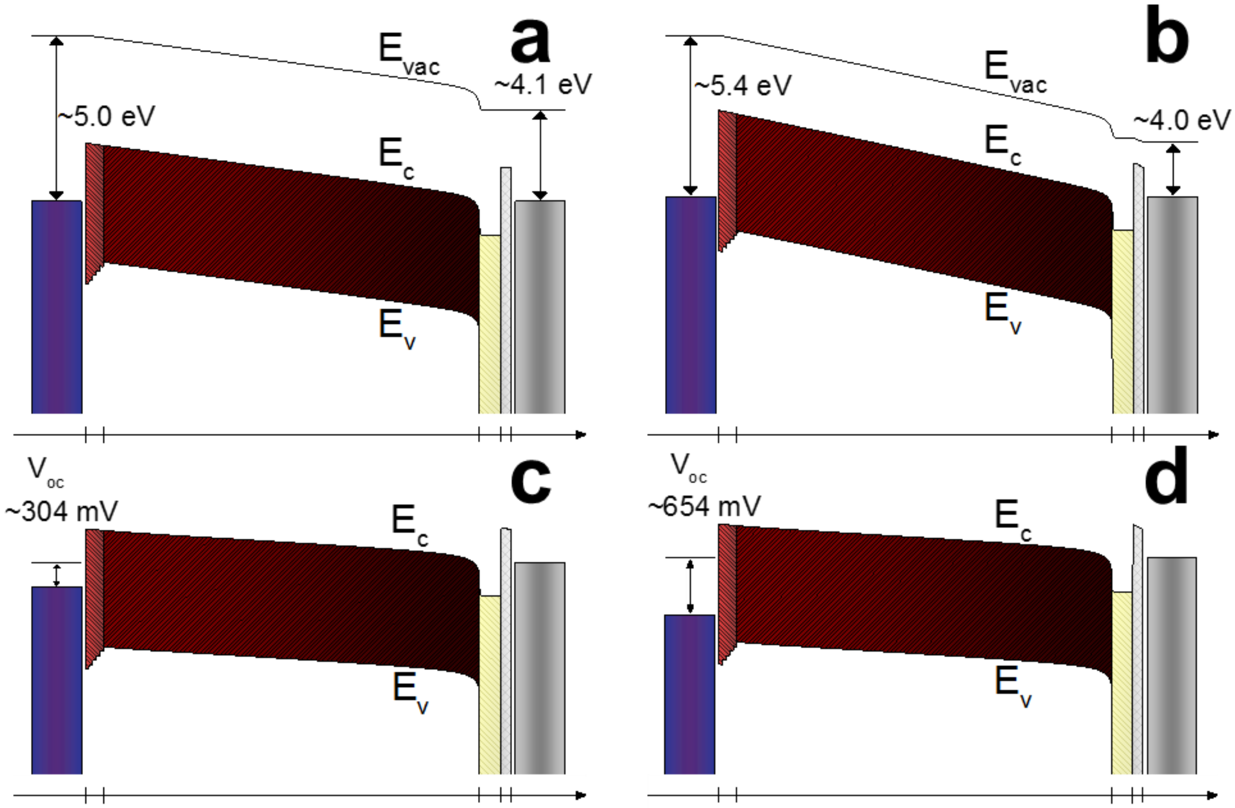

Figure 3.9. Band diagrams of modeled CdTe solar cells with ITO/"CdTeO$_x$"/CdTe/ZnO/"AlO$_x$"/Al geometry at equilibrium (a,b) and V_{oc} (c,d) before (a,c) and after (b,d) current/light soaking. Input parameters can be found in the Supplemental Information.

From the device parameters inputted, the work function of ITO is approximated at ~5.0 eV before current/light soaking (Figure 3.9a). Normally, the work function of ITO ranges from 4.8-5.0 eV based on manufacturer specifications (Thin Film Devices Inc.). The modeled work function lies on the deeper side of the range, which agrees with previous reports.[24-25] Oxygen plasma cleaning, the treatment used to hydrophilize the substrates in preparation of spincoating, was shown to deepen the work function of ITO by removing surface adsorbates. Ding et al. found the work function of ITO was actually even lower, ~5.2 eV.[24] We modeled heavily doped CdTe at the interface between ITO and the CdTe absorber layer to determine if such a method would improve V_{oc} (Figure 3.10b,d). It improved by over 300 mV, indicating such a method might be useful in forming a transparent Ohmic contact to CdTe.

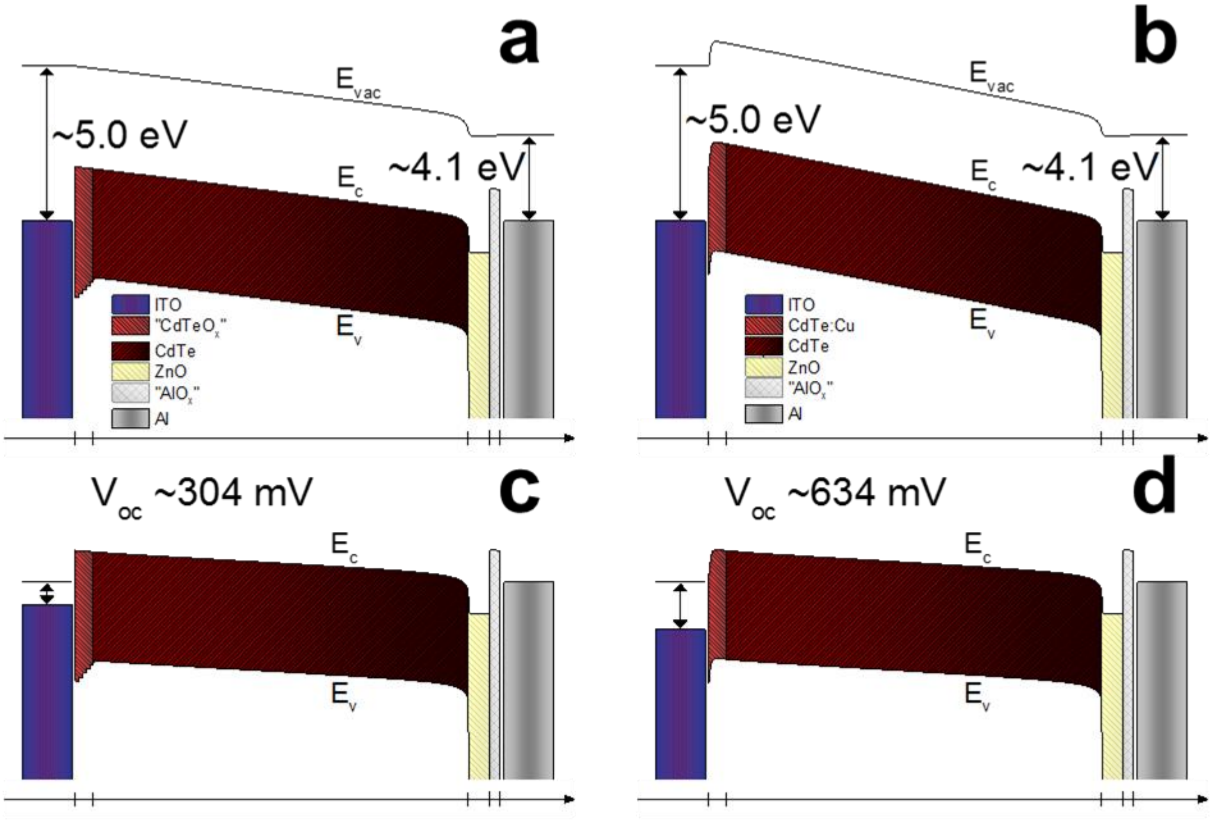

Figure 3.10. (a,c) Band diagrams of modeled CdTe solar cells with ITO/”CdTeOx”/CdTe/ZnO:In/”AlOx”/Al geometry at equilibrium (a) and V_{oc} (c) before current/light soaking. (b,d) Band diagrams of modeled CdTe solar cells with CdTe:Cu with 10^{19} cm^{-3} N_A layer between ITO and CdTe at equilibrium (b) and V_{oc} (d) before current/light soaking. Input parameters can be found in Supporting Information.

3.5. Low temperature current-voltage sweeps.

The current plateau observed in forward bias (Figure 3.11a) under illumination is called rollover. Rollover occurs when one (or both) of the majority carriers are difficult to extract from the device stack. Usually, if both carriers are difficult to extract, the device performance suffers greatly. It is widely considered that rollover is caused by poor carrier collection dictated by thermionic emission (Equation 3.1).[37]

$$J_t = A^* T^2 e^{\frac{-q\Phi_b}{kT}} \tag{3.1}$$

where J_t is saturation current, A^* is the Richardson constant, T is temperature, q is the charge of an electron, Φ_b is the barrier potential, and k is Boltzmann's constant.

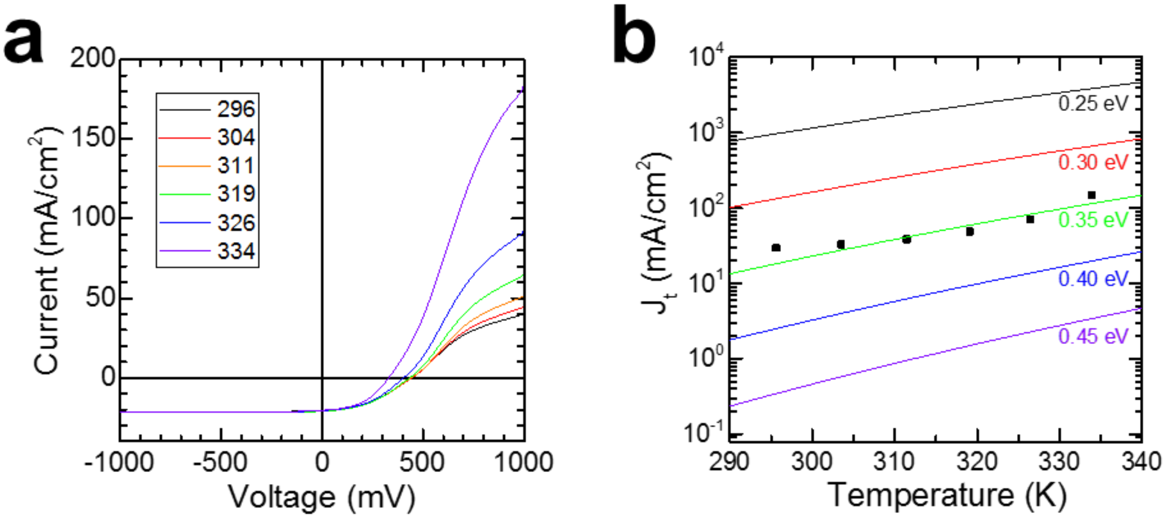

Figure 3.11. (a) JV curves under approximated AM1.5G illumination taken at 296 K (black), 304 K (red), 311 K (orange), 319 K (green), 326 K (blue), and 334 K (purple). (b) J_t versus temperature plot with Φ_b equal to 0.25 eV (black), 0.30 eV (red), 0.35 eV (green), 0.40 eV (blue), and 0.45 eV (purple) with the Richardson constant set to 222.6 $mA/cm^2/K^2$ above RT.

JV curves under approximated AM1.5G illumination over a range of temperatures (Figure 3.11a) were taken to calculate a potential barrier. As the temperature increases, the barrier became less effective at blocking carriers from being captured, causing rollover to lessen. J_t was determined by applying a fit to the two regimes of linearity for each curve and calculating the intersection point (Figure 3.12). The potential barrier can be calculated by linearizing the relationship between J_t and T (Equation 3.2).

$$\ln\left(\frac{J_t}{T^2}\right) = \frac{-q\,\Phi_b}{k}\,\frac{1}{T} + \ln(A^*) \tag{3.2}$$

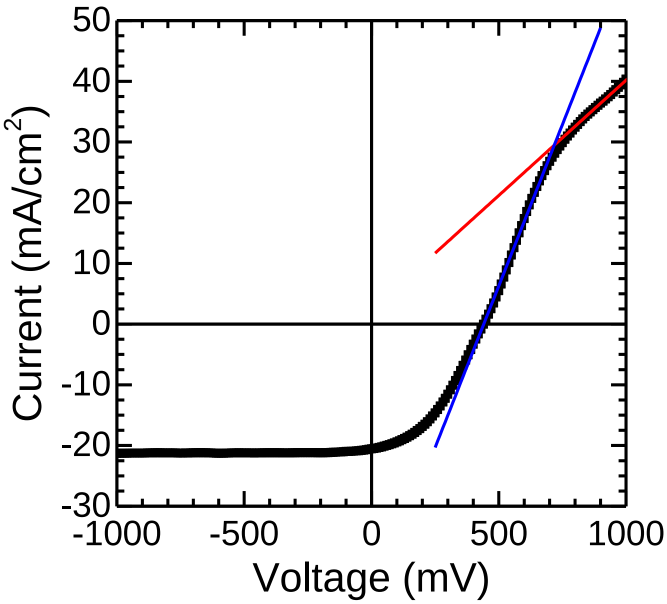

Figure 3.12. JV curve under AM1.5G illumination of the control device without current/light soaking at RT illustrating the linear fit of the top (red) and bottom (blue) portion of saturation current extraction.

By plotting $\ln\left(\frac{J_t}{T^2}\right)$ vs. $\frac{1}{T}$, the slope and y-intercept become $\frac{-q\,\Phi_b}{k}$ and $\ln(A^*)$, respectively. Linear fits using this method tend to overemphasize the lower temperature points by decreasing their relative contribution to variance. The Richardson constant (222.6 mA/cm^2/K^2) for every curve was kept constant and only Φ_b was varied (Figure 3.11b). As Φ_b increases, J_t will decrease significantly as well. The approximation of ~0.35 eV closely matches with the experimental data.

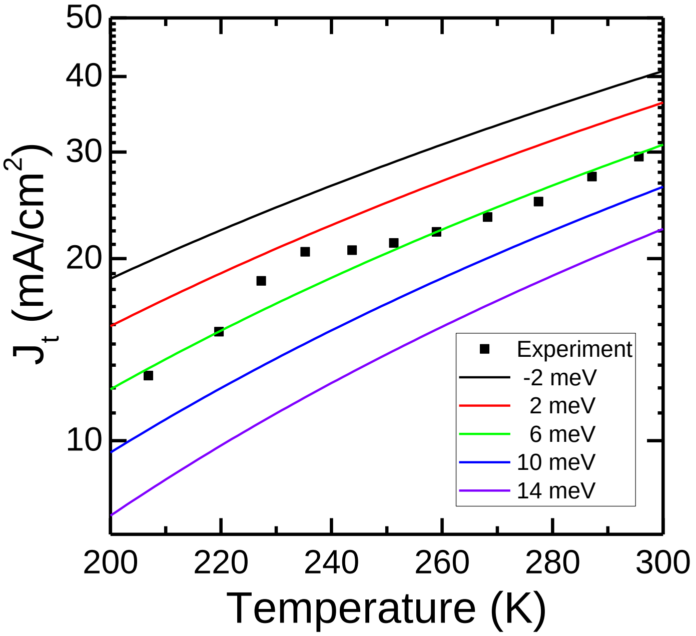

Figure 3.13. J_t versus temperature plot with Φ_b equal to -2 meV (black), 2 meV (red), 6 meV (green), 10 meV (blue), and 14 meV (purple) with the Richardson constant set to 0.436 μA/cm^2/K^2 below RT.

A new Richardson constant (0.436 μA/cm^2/K^2) was calculated and applied to the curves below RT (Figure 3.13). At ~240 K, there are a couple of outliers, but the fit matches well overall. A difference of regimes can be explained by inconsistencies in the device stack.

3.6. Interfacial layers to improve photovoltaic performance.

There are three major attributes interfacial layers (Figure 3.14a) must possess to become applicable contacts to CdTe: transparent, stable, and form an Ohmic contact to p-type CdTe. Interfacial layers must allow light to pass so the CdTe absorber layer can generate electron-hole pairs. They must also be stable over long periods of time to prevent considerable device degradation, otherwise current/light soaking would be a preferred option. Finally, interfacial layers must possess a deep work function (Fermi level) so as to prevent a Schottky-like contact to CdTe. We found etched CdTe:Cu, Te, and ZnTe:Cu worked well as interfacial layers.

3.6.1. Iodide/triiodide etched copper-doped cadmium telluride.

An ideal candidate for creating an Ohmic contact to CdTe is heavily p-type CdTe (Figure 3.10b,d). There would be no differences in the conduction or valence bands, no issues with materials incompatibility, and no adverse side reactions since it is the same material. Modeling of heavily doped CdTe located at the ITO/CdTe interface shows it could work to improve V_{oc}. Attempts at creating heavily doped CdTe made by adding Cu-containing salts alone proved ineffective at improving V_{oc}. Most likely, Cu diffused out of the initial layer through the grain boundaries during the deposition of the CdTe absorber layer. In an attempt to prevent Cu from diffusing away from the ITO/CdTe interface, a saturated solution of NH_4I in IPA was used to impregnate the film with I^-. I^- was shown to inhibit grain growth, which requires recrystallization to combine smaller grains into larger ones.[38] Diffusion requires the same recrystallization processes, so the intention was to use I^- to keep Cu in the interfacial layer. However, by simply soaking in a saturated NH_4I solution, V_{oc} did not improve (black, Figure 3.14b).

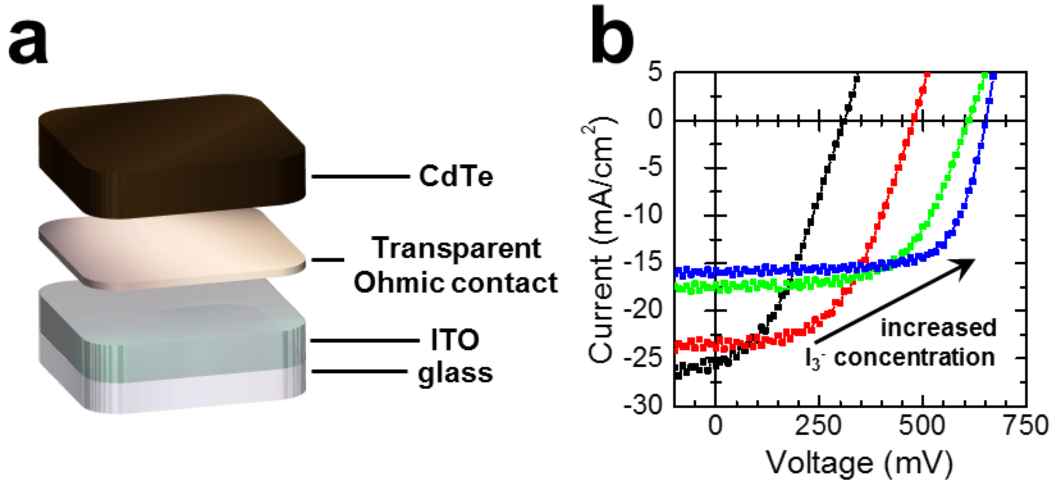

Figure 3.14. (a) Schematic of the interfacial layer approach. (b) JV curves under AM1.5G illumination for interfacial layer devices using etched CdTe:Cu. CdTe:Cu was deposited and soaked for 10 minutes in I^-/I_3^- with 0% (black), 0.25% (red), 0.375% (green), and 0.5% (blue) I_2 added to saturated NH_4I solution in IPA followed by CdTe absorber layer deposition.

Another approach to forming Ohmic contact to CdTe is through a 10 volume% iodine/methanol etch.[39] Along with pure saturated NH_4I solution, 0.375% I_2 solution in IPA was added to the NH_4I solution and used to soak the first layer. Mixing I_2 and I^- forms I_3^- in-situ, indicated by a peak in UV-vis absorption at ~360 nm (Figure 3.15a) and the solution turning yellow (Figure 3.15b).[40] The samples were all soaked for 10 minutes to test how the etch concentration affects contact to ITO. An increase in I_3^- concentration increases the etch rate, which will make the material more Te-rich. None of the samples with I_2 added required current/light soaking to achieve larger V_{oc}'s (Figure 3.14b).

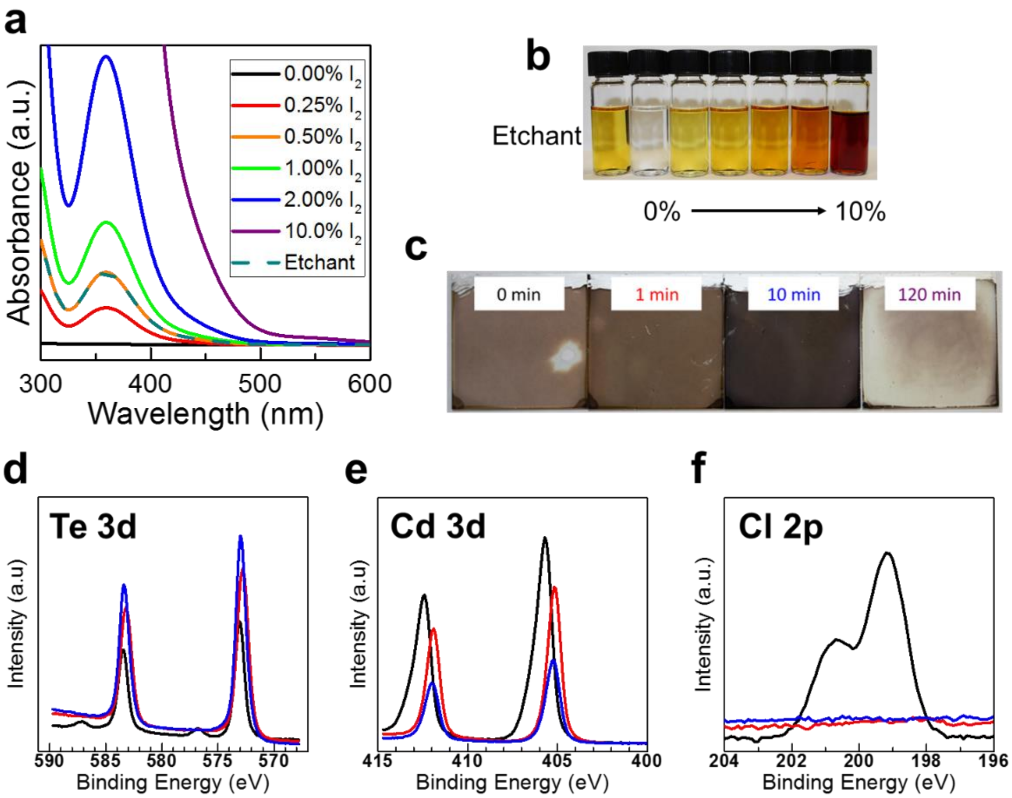

Figure 3.15. (a) UV-vis spectra of diluted I^-/I_3^- solution showing increased absorption at ~360 nm with increasing I_3^- concentration. (b) Image of vials containing (from left to right) the etchant, 0%, 0.25%, 0.5%, 1%, 2%, and 10% I_2 added to saturated N_4I solution in IPA. (c) Image (from left to right) of etched CdTe:Cu films etched for 0, 1, 10, and 120 minutes soaked in saturated NH_4I in IPA with 0.375% I_2 added. (d-f) XPS spectra comparing 0 (black), 1 (red), and 10 minutes (blue) etched CdTe:Cu films soaked in saturated NH_4I in IPA with 0.375% I_2 added in Te 3d (d), Cd 3d (e), and Cl 2p (f) regions.

Concentration is only one method of adjusting the properties of the final layer. Time can be used to control to what extent the etch proceeds. Cd 3d, Te 3d, and Cl 2p XPS were performed on etched CdTe:Cu soaked for 0 (black), 1 (red), 10 (blue), and 120 minutes in 0.375% I_2 added to saturated NH_4I in IPA. XPS helps determine time scales for each step of the etch (Figure 3.15d-f). The Te (Figure 3.15d) concentration relative to Cd (Figure 3.15e) increases with longer etch times. Most likely, Cd is solubilized by I^- and removed from the film. Additionally, the extra peaks in the original Te XPS trace (black, Figure 3.15d) disappear. Previous accounts attribute those peaks to oxidized Te (TeO_2).[41] Finally, all traces of Cl (black, Figure 3.15f) are removed within the first minute of the soak, indicating solubilization of surface $CdCl_2$. The likely explanation for these phenomena is reduction of TeO_2 with NH_4I (Equation 3.3) and oxidation of CdTe to Te with Cd being solubilized (Equation 3.4). Also, a well-known reaction between Cu(II) and I^- should take place (Equation 3.5).

$$(3.3)\quad TeO_2(s) + 4NH_4^+ + 6I^- \rightarrow Te(s) + 2H_2O + 2I_3^- + 4NH_3$$

$$(3.4)\quad CdTe(s) + I_3^- \rightarrow Te(s) + Cd^{2+} + 3I^-$$

$$(3.5)\quad 2Cu^{2+} + 5I^- \rightarrow 2CuI + I_3^-$$

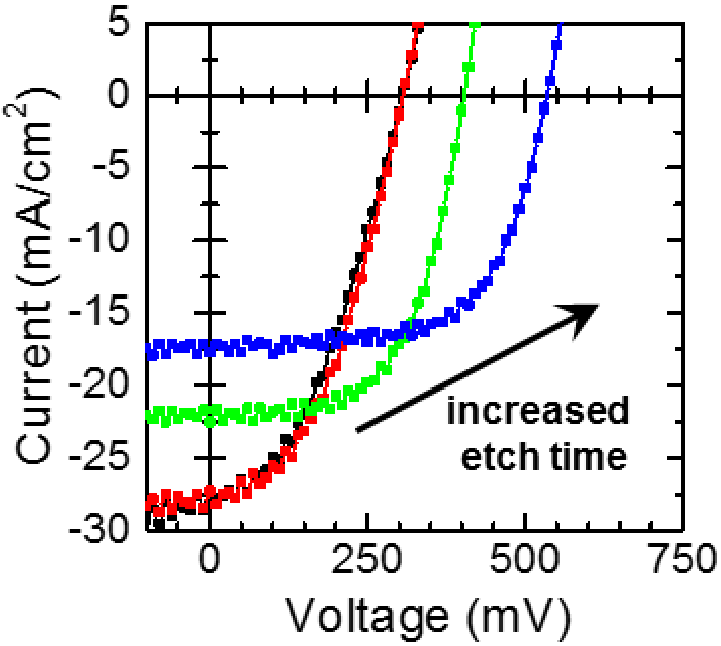

Figure 3.16. JV curves of with CdTe solar cells under AM1.5G illumination. Cells were made using etched CdTe:Cu interfacial layer devices with 0.375% I_2 added to saturated NH_4I in IPA soaked for 0 (black), 1 (red), 3 (green), and 5 (blue) minutes followed by CdTe absorber deposition.

V_{oc} increased, to a point, with a longer etch time (Figure 3.16a). Eventually, the entire CdTe film can be dissolved (120 minutes, Figure 3.15c). Devices made with etched CdTe:Cu interfacial layer yielded efficiencies of ~7.0% for PCE with 514 mV, 21.9 mA/cm^2, and 63% for V_{oc}, J_{sc}, and FF, respectively. Average values on one substrate were ~6.1% for PCE with ~510 mV, ~19.3 mA/cm^2, and ~63% for V_{oc}, J_{sc}, and FF, respectively. The largest discrepancies lie with J_{sc}, which is typical of the methods employed for CdTe deposition. With better control over processing conditions, devices are expected to become more efficient and consistent.

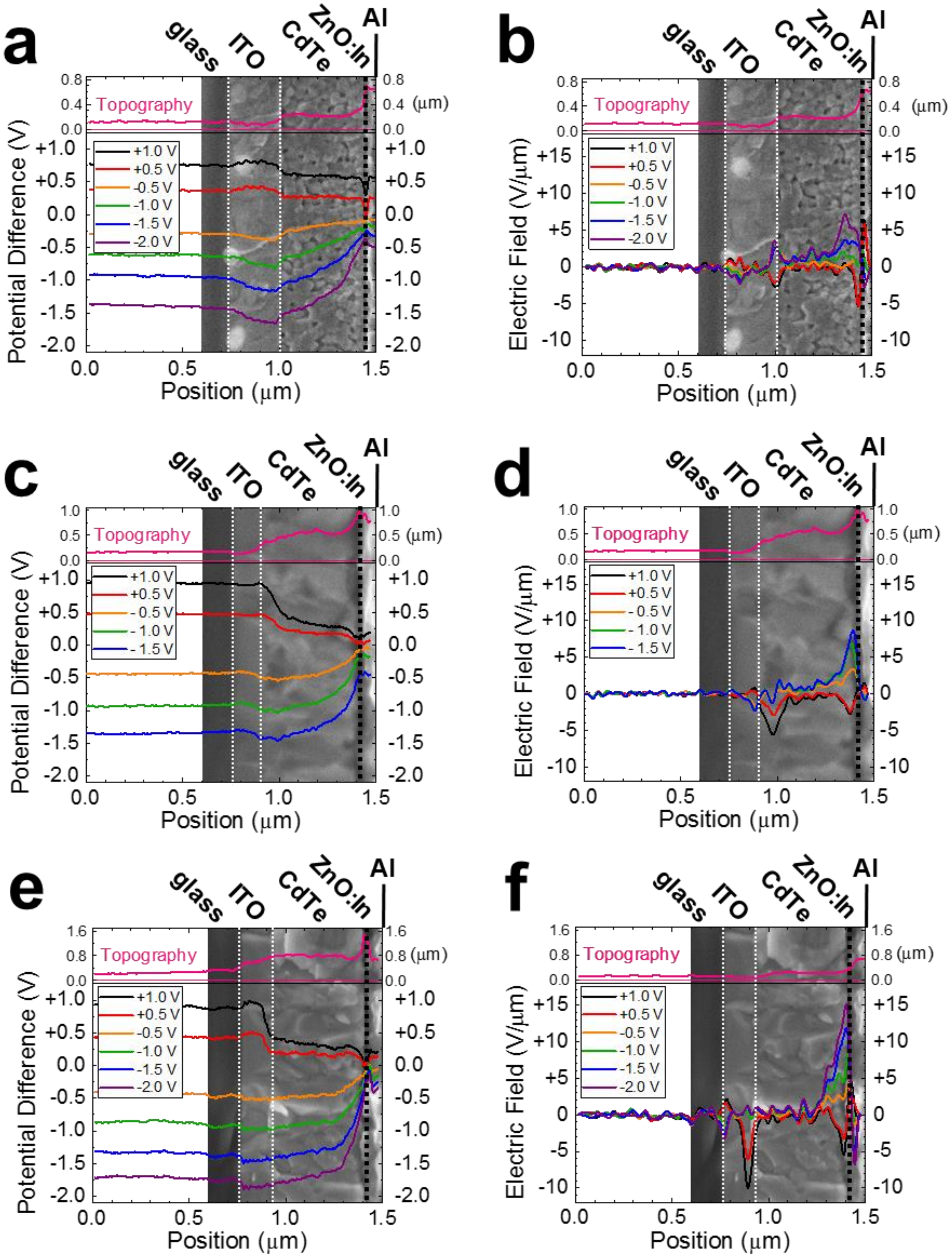

Figure 3.17. SKPM data showing the topography (pink) with the normalized scans at +1 V (black), +0.5 V (red), -0.5 V (orange), -1.0 V (green), and -1.5 V (blue) bias across the device. (a,b) SKPM scans showing the normalized potential difference (a) and the normalized electric field (b) at the varied device biases for the control device. (c,d) SKPM scans showing the

Figure 5.17 (cont'd) normalized potential difference (c) and normalized electric field (d) at the varied device biases for the 1 minute etched CdTe:Cu interfacial layer device using 0.375% I_2 added to saturated NH_4I in IPA. (e,f) SKPM scans showing the normalized potential difference (e) and the normalized electric field (f) at the varied device biases for the etched CdTe:Cu interfacial layer device etched for 5 minutes with 0.375% I_2 added to saturated NH_4I in IPA.

Etched CdTe:Cu interfacial layer devices etched for 1 and 5 minutes with 0.375% I_2 added to saturated NH_4I in IPA along with the control device were measured using cross-sectional SKPM (Figure 3.17). Both the control device (green, Figure 3.17b) and 1 minute etched CdTe:Cu (green, Figure 3.17d) devices showed a potential change at the ITO/CdTe interface under reverse bias. However, with the 5 minute etched CdTe:Cu (green, Figure 3.17f) device, the feature is absent. V_{oc} is improved significantly, ~250 mV, for the device etched for 5 minutes, so an absence of the potential drop agrees with device improvement. Under forward bias, there is a large potential drop for the device etched for 5 minutes (black, Figure 3.17f). Etched CdTe:Cu works as an interfacial layer by more easily extracting holes under illumination. This would make extracting electrons more difficult, which ITO needs to do under forward bias. It is believed the sharp drop at the CdTe/ZnO:In interface under reverse bias (green, Figure 3.17f) occurs because CdTe is locally doped by the interfacial layer. Doping of the CdTe absorber layer shortens the depletion region, which causes the potential drop to occur in a narrower area. If the field does not span the entire CdTe layer, then electrons and holes would need to diffuse to the contacts, increasing the likelihood of recombination. This can explain the loss of J_{sc} as etch time increases (Figure 3.16).

3.6.2. Spincoated tellurium from hydrazine.

Another approach to the formation of transparent Ohmic contact to CdTe involved a thin layer of Te. Te can be solution-processed from polytelluride (Te_n^{2-}) ions dissolved in N_2H_4 (Equation 3.6).

$$2n \cdot Te + 5N_2H_4 \rightarrow\ 4N_2H_5^+ + 2Te_n^{2-} + N_2 \tag{3.6}$$

N_2H_4 can reduce Te to Te_n^{2-}, but not fully to Te^{2-}, giving the solution a deep purple color.[42] Upon spincoating and annealing at 200 °C, the purple Te_n^{2-} solution transitions back to elemental Te. The CdTe NC solution wets the surface of the Te layer, so the CdTe absorber layer is easy to deposit on top to finish the device stack. By varying the concentration of Te in N_2H_4, the thickness of the interfacial layer can be changed, influencing the overall device performance (Figure 3.18). Mott-Schottky analysis (Figure 3.18b) illustrates the improvement in built-in potential (V_{bi}) of the as-made devices, leading to an increase in V_{oc}. Lines of the linear region were drawn to estimate V_{bi} by extending them to the x-intercept. The estimations for V_{bi} match closely to measured V_{oc}'s (Table 3.VI). Differences between V_{bi} and V_{oc} arise from discrepancies with the linear fit in Mott-Schottky measurements as well as differences in the measurements themselves. Since Mott-Schottky are taken in the dark versus JV being taken under AM1.5G illumination, there are subtle differences in the potential differences measured. Te layers that are too thick result in reduced J_{sc} because Te absorbs light.[43]

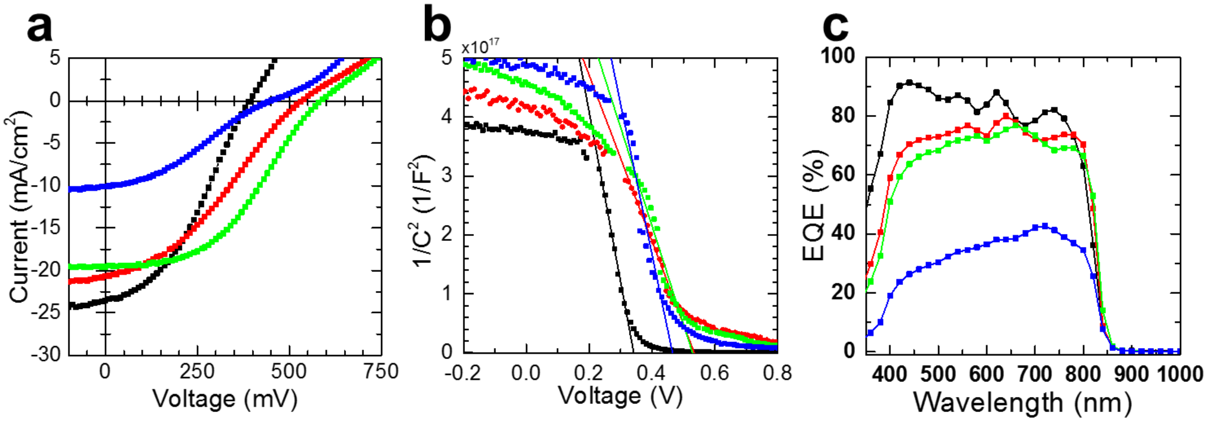

Figure 3.18. JV curves under AM1.5G illumination (a), Mott-Schottky (b), and EQE (c) measurements for interfacial layer devices using spincoated Te from N_2H_4. 0.1M (black), 0.2M (red), 0.3M (green), and 0.5M (blue) Te in N_2H_4 was spincoated at 2000 rpm onto ITO-coated glass and annealed at 200 °C for 30 minutes followed by CdTe absorber layer deposition. Lines for Mott-Schottky were extrapolated to zero to estimate V_{bi}.

Table 3.VI. Built-in potential and open circuit voltages for interfacial layer devices utilizing spincoated Te.

Te Molarity	V_{bi}	V_{oc}
0.1 M Te	342	392
0.2 M Te	534	533
0.3 M Te	529	596
0.5 M Te	465	548

By measuring EQE (Figure 3.18c), it becomes clear making the Te layer thicker increasingly attenuates the light reaching the CdTe layer. The differences in J_{sc} follow the same trends in EQE. As the Te layer gets thicker, EQE drops, but more dramatically with green light (~500 nm).

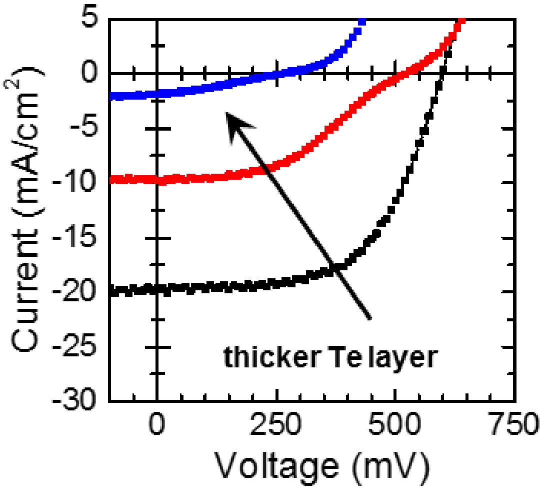

Figure 3.19. JV curves under AM1.5G illumination for interfacial layer devices using Te dissolved in N_2H_4. 0.1M (black), 0.5M (red), and 1.0M (blue) Te in N_2H_4, spincoated at 3000 rpm onto ITO-coated glass and annealed at 350 °C for 30 minutes followed by CdTe absorber layer deposition.

By increasing the spincoating speed to 3000 rpm and changing the annealing temperature to 350 °C, JV characteristics improved (Figure 3.19). Increasing spincoating speed thinned the layer to allow more light to reach CdTe and increasing the annealing temperature makes the Te layer more crystalline. Te is less likely to diffuse through the grain boundaries in a crystalline state over an amorphous state. FF was significantly improved from a decrease in series resistance, as seen by the slope at V_{oc}. By exploring different processing conditions, the device performance can be even higher. Devices with spincoated Te yielded efficiencies of ~7.0% for PCE with 597 mV, 19.7 mA/cm^2, and 59% for V_{oc}, J_{sc}, and FF, respectively. Average values on one substrate were ~6.1% for PCE with ~597 mV, ~19.0 mA/cm^2, and ~52% for V_{oc}, J_{sc}, and FF, respectively. The largest differences once again were from J_{sc}.

3.6.3. Etched copper-doped cadmium telluride and spincoated tellurium longevity.

V_{oc} for I^-/I_3^- etched CdTe:Cu and spincoated Te remained high through the course of a week without considerable change (Figure 3.20). Long term degradation of device performance can be partially attributed to the formation of an intermetallic between Al and Ag. Pfeifer et al. observed a degradation of Ag-coated Al electrical contacts over time attributed to the formation of resistive intermetallics, Ag_2Al and Ag_3Al.[44] All devices we made with the Al/Ag interface degrade in such a manner. However, V_{oc} changed little, indicating etched CdTe:Cu and spincoated Te created stable Ohmic contacts over longer periods of time than current/light soaking.

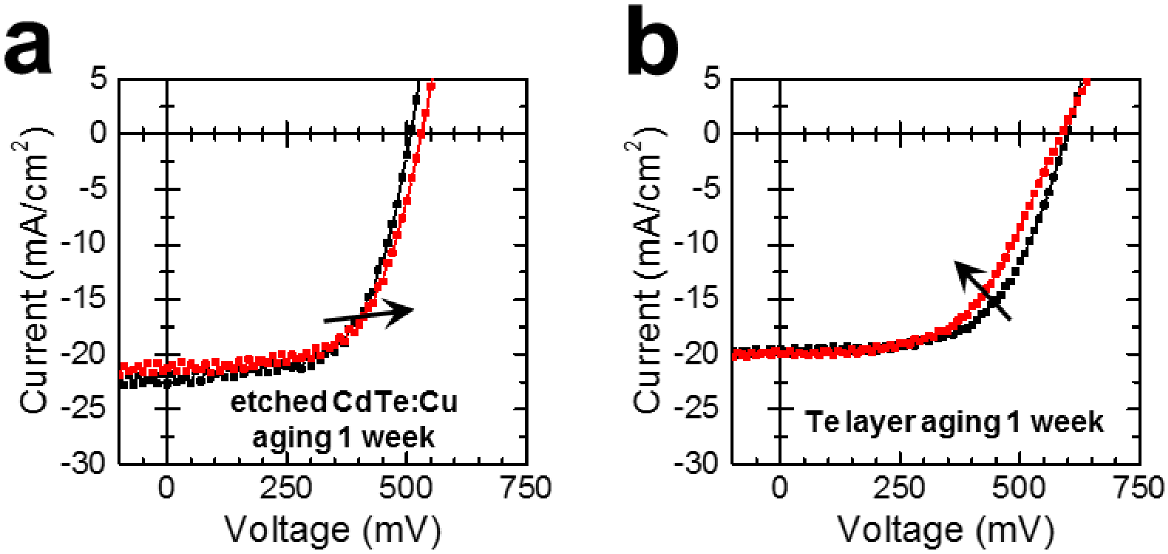

Figure 3.20. (a) JV curves under AM1.5G illumination for 0.375% I_2 added to saturated NH_4I etched CdTe:Cu etched for 5 minutes interfacial layer device immediately after fabrication (black) and aged for 1 week (red). (b) JV curves under AM1.5G illumination for spincoated at 3000 rpm 0.1M Te in N_2H_4 annealed at 350 °C for 30 minutes interfacial layer device immediately after fabrication (black) and aged for 1 week (red).

3.6.4. Copper- or silver-doped cadmium telluride.

Attempts at simply adding Cu salts to the CdTe NC ink failed to produce an appreciable difference in device performance (red, Figure 3.21). Cu most likely diffused through the grain boundaries, removing substantial amounts of Cu from the ITO/CdTe interface. Ag nanowires (blue, Figure 3.21) completely shorted the device. Electroplated Cu failed to improve contact between ITO and CdTe (green, Figure 3.21). J_{sc} was probably diminished by a combination of mirroring and oxidation. Depositing Cu in the form of Cu_2Te NCs proved to be a viable method for improving contact between ITO and CdTe (black, Figure 3.21). By trapping Cu in a lattice instead of pushing it to the grain boundaries, the V_{oc} improved dramatically. The best device yielded PCE as high as ~8.6% for PCE with 685 mV, 21.3 mA/cm^2, and 59% for V_{oc}, J_{sc}, and FF, respectively. Unfortunately, this method proved to rather inconsistent. Further optimization will be necessary to improve batch-to-batch reproducibility.

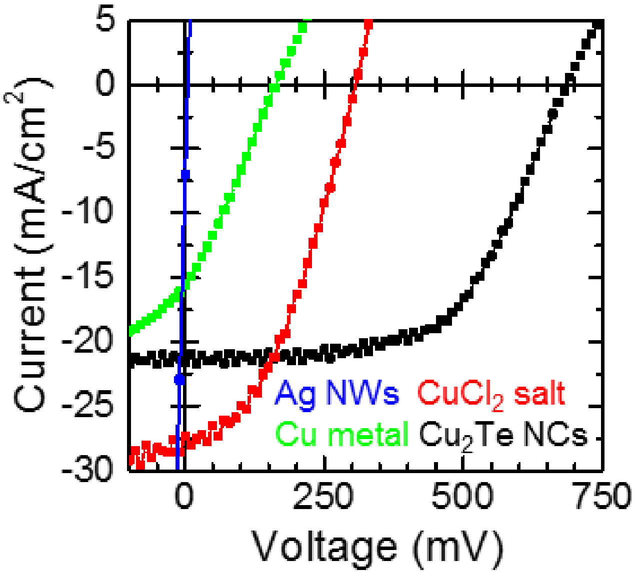

Figure 3.21. JV curves under AM1.5G illumination without current/light soaking for interfacial layers using Cu or Ag to dope CdTe. Cu_2Te NCs added to CdTe NCs (black), $CuCl_2$ added to CdTe NCs (red), Cu electrochemically deposited (green), or Ag NWs spincoated (blue) onto ITO-coated glass for the first layer followed by CdTe absorber deposition.

3.6.5. Sputtered copper-doped zinc telluride.

Since it has already found use for Ohmic contacts in conventional devices, another possible material for creating a transparent Ohmic contact to CdTe is ZnTe:Cu. It has a wider band gap (2.35 eV) than CdTe and is more easily doped p-type with Cu.[45] With its conduction band above that of CdTe, ZnTe acts as an electron blocking layer, preventing recombination at the back contact. All of these factors make ZnTe:Cu a possible interfacial layer. A sputtered layer of copper-doped zinc telluride (Figure 3.22) proved effective at improving V_{oc}.

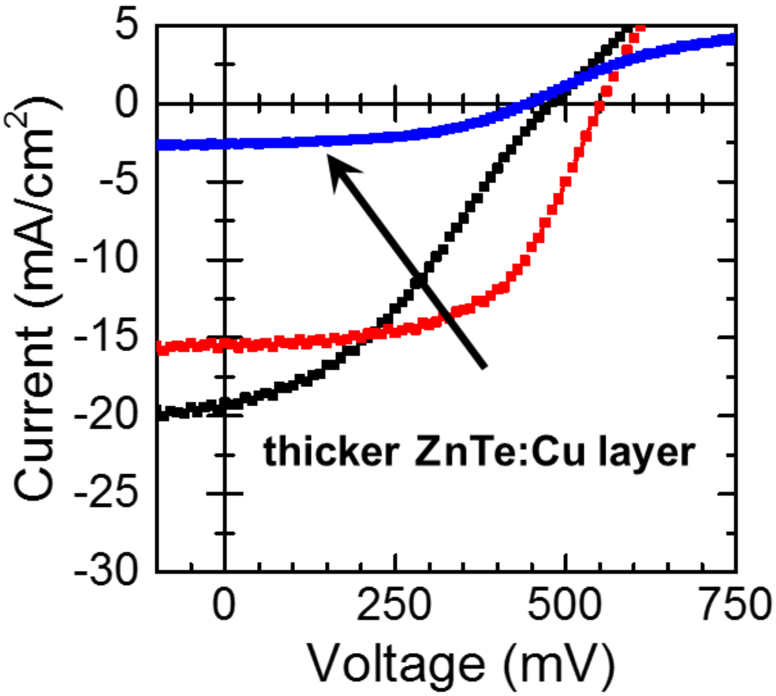

Figure 3.22. JV curves under AM1.5G illumination for interfacial layer devices using sputtered ZnTe:Cu. 10 nm (black), 20 nm (red), and 40 nm (blue) ZnTe: was sputtered onto ITO-coated glass followed by CdTe absorber layer deposition.

Increasing the thickness of ZnTe:Cu increases V_{oc} to a point. The ZnTe:Cu layer was sputtered and used as-made with no additional treatments. The surface roughness of sputtered materials tends to be larger than spincoated films. If the surface roughness is on the order of the film thickness, then layer consistency will considerably affect the average device performance. This method proved to be less consistent than either etched CdTe:Cu or spincoated Te. The best device achieved PCE of ~4.8% with 552 mV, 15.5 mA/cm^2, and 57% for V_{oc}, J_{sc}, and FF, respectively. Average values on one substrate were ~3.0% for PCE with ~464 mV, ~12.5 mA/cm^2, and ~50% for V_{oc}, J_{sc}, and FF, respectively. With a number of additional treatments, the overall device performance can improve further. For instance, the layers could be annealed before addition of the CdTe absorber layer to improve series resistance. SKPM showed ZnTe:Cu (Figure 3.23) interfacial layer devices demonstrated similar device response to etched CdTe:Cu soaked for 5 minutes.

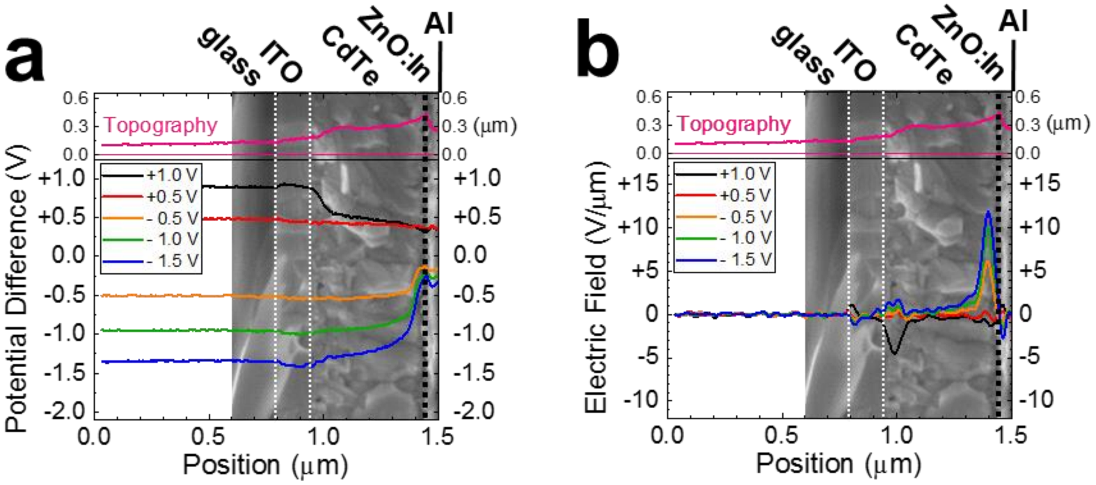

Figure 3.23. SKPM data showing the topography (pink) with the normalized scans at +1 V (black), +0.5 V (red), -0.5 V (orange), -1.0 V (green), and -1.5 V (blue) bias across the device. (a,b) SKPM scans showing the normalized potential difference (a) and normalized electric field (b) at the varied device biases for the 20 nm ZnTe:Cu interfacial layer device with 2 wt% Cu added.

3.6.6. Spincoated zinc telluride from hydrazine.

Solution-processed ZnTe:Cu was attempted by starting with $(N_2H_4)_2ZnTe$ prepared using the methods outlined by Mitzi et al.[35] Adding Cu to N_2H_4 had its own challenges. N_2H_4 is a strong enough reducing agent to reduce Cu in CuCl to Cu metal, making solubilizing Cu halide salts difficult. Acetonitrile coordinates to Cu(I) metal centers well enough to prevent reduction, but it is not strong enough to prevent a reaction between Cu(I) and ZnTe. A brown suspension developed from the formation of Cu_2Te as the two solutions were mixed. Cu is not the only element to dope ZnTe. Romeo et al. showed Sb can dope ZnTe p-type by lying on the Te site of the lattice.[46] Kovalenko et al. determined a preparation for Sb_2Te_3-N_2H_4, which mixes with $(N_2H_4)_2ZnTe$ without reacting.[34] By adding enough, V_{oc} can improve to as high as 573 mV (Figure 3.24). However, J_{sc} decreases substantially, making PCE even lower than the control device without current/light soaking.

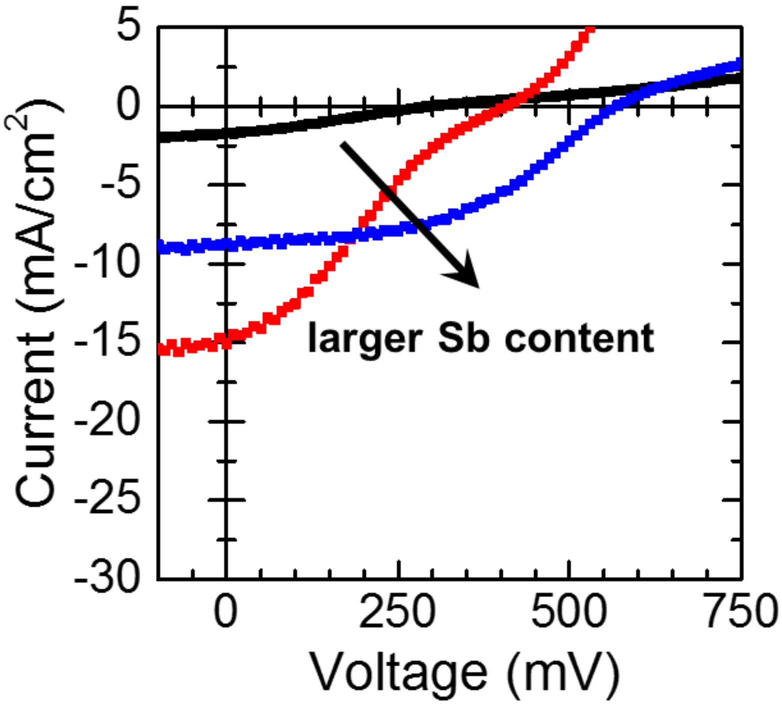

Figure 3.24. JV curves under AM1.5G illumination without current/light soaking for interfacial layers using spincoated ZnTe. 0% (black), 1% (red), and 10% (blue) by mole Sb_2Te_3-N_2H_4 added to $(N_2H_4)_2ZnTe$ was spincoated onto ITO-coated glass and annealed at 200 °C for 30 minutes followed by CdTe absorber deposition.

Interestingly, current/light soaking still improves V_{oc} in the lower Sb_2Te_3-N_2H_4 content interfacial layer devices (Figure 3.25). The overall device performance improved for both cases, but more noticeably for the device with Sb_2Te_3-N_2H_4 added. $(N_2H_4)_2ZnTe$ alone was too resistive to improve greatly with current/light soaking. However, a slight addition of Sb_2Te_3-N_2H_4 added to $(N_2H_4)_2ZnTe$ before spincoating significantly improved V_{oc} from ~650 mV for the control device to ~ 730 mV the spincoated ZnTe interfacial layer device after current/light soaking. V_{oc} likely improved compared to the control because ZnTe acted as an electron blocking layer. J_{sc} and FF remain relatively low, most likely from an increase in series resistance.

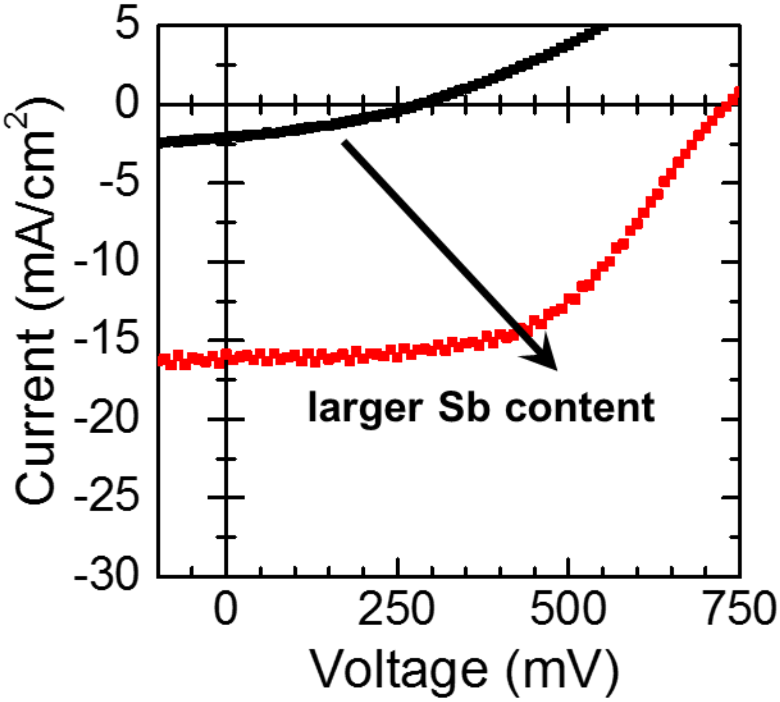

Figure 3.25. JV curves under AM1.5G illumination after current/light soaking for interfacial layers using spincoated ZnTe. 0% (black) and 1% (red) by mole Sb_2Te_3-N_2H_4 added to $(N_2H_4)_2ZnTe$ was spincoated onto ITO-coated glass and annealed at 200 °C for 30 minutes followed by CdTe absorber deposition.

3.6.7. Spincoated tellurocadmate-capped cadmium telluride nanocrystals.

Dolzhnikov et al. synthesized new ligands for CdTe NCs that closely match the composition, preventing a large inclusion of impurities.[36] A_2CdTe_2 (where A = Na^+, K^+, Cs^+, and $N_2H_5^+$) functionalizes the surface of CdTe NCs and creates a solution that can be spincoated onto ITO-coated glass. Changing the cation (A^+) changes the overall properties of the layer by changing doping, diffusivity, and overall consistency of the deposited layer. The alkali metal cations do not breakdown, but $(N_2H_5)_2CdTe_2$ should follow a similar decomposition process to $(N_2H_5)_2Te_n$

(reverse of Equation 3.6). In all cases, none of the layers effectively created a transparent Ohmic contact to CdTe, but an interesting trend in device performance occurred upon current/light soaking (Figure 3.26).

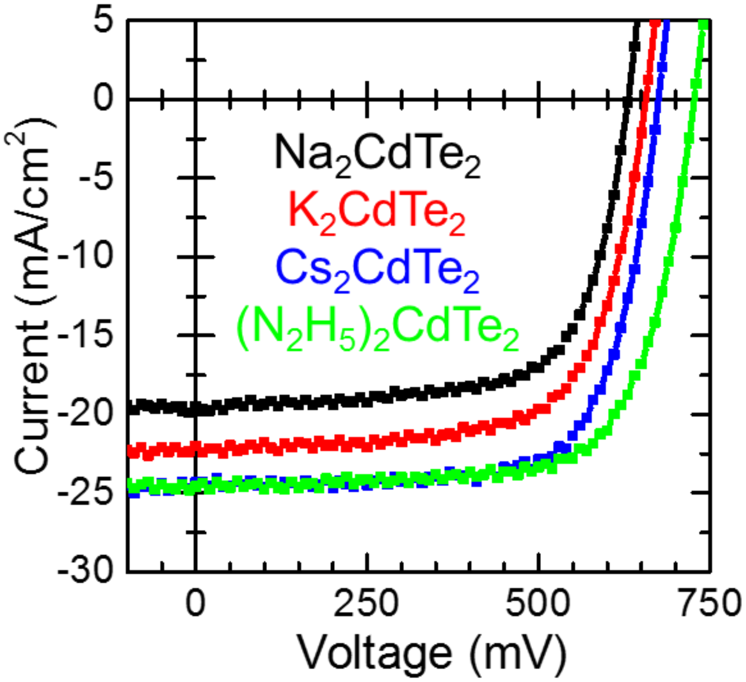

Figure 3.26. JV curves under AM1.5G illumination after current/light soaking for interfacial layers using A_2CdTe_2-capped NCs. Na_2CdTe_2- (black), K_2CdTe_2- (red), Cs_2CdTe_2- (blue), and $(N_2H_5)_2CdTe_2$-capped CdTe NCs at a concentration of 60 mg/mL were spincoated at 2000 rpm onto ITO-coated glass and annealed at 350 °C for 30 minutes followed by CdTe absorber deposition.

The device performance improves as the alkali cation size increases. Smaller elements diffuse more rapidly through the grain boundaries. Alkali cations diffusing into the subsequent CdTe absorber layer will likely dissolve into the $CdCl_2$ bath along with chloride. Dissolution of ACl (where $A^+ = Na^+$, K^+, and Cs^+) will decrease grain boundary passivation, increasing the chance of electron-hole pair recombination in the device. $N_2H_5^+$ cannot diffuse away, because it breaks down to leave Te-rich CdTe. Te diffuses slightly, but not nearly as much as the alkali metal cations. Interestingly, CdTe/$(N_2H_5)_2CdTe_2$ as an interfacial layer improved V_{oc} to ~725 mV without decreasing J_{sc}. The best device achieved PCE of ~12.7% with 726 mV, 24.6 mA/cm^2, and 71% for V_{oc}, J_{sc}, and FF, respectively. Typical values on one substrate were ~11% for PCE with ~700 mV, ~23 mA/cm^2, and ~70% for V_{oc}, J_{sc}, and FF, respectively. While CdTe/$(N_2H_5)_2CdTe_2$ does not create an Ohmic contact, it can be useful in combination with layers that do.

3.7. Comparison of transparent Ohmic contacts to cadmium telluride.

We described a variety of methods for improving V_{oc} without the need for current/light soaking. Many of the methods use solution-processing and are easily integrated into typical device fabrication processes.

Table 3.VII. Compiled table of device performance without current/light soaking.

Devices With No Current/Light Soaking

Interfacial Layer	PCE (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
No Interfacial Layer (best)	4.0	385	24.5	38
(typical)	3.3	350	24.0	39
Etched CdTe:Cu (best)	7.0	514	21.9	63
(typical)	6.1	510	19.3	63
Spincoated Te (best)	7.0	597	19.7	59
(typical)	6.1	597	19.0	52
Sputtered ZnTe:Cu (best)	4.8	552	15.5	57
(typical)	3.0	464	12.5	50
CdTe:Cu from $Cu(I)_2Te$ NCs (best)	8.6	685	21.3	59
Spincoated “ZnTe:Sb” (best)	2.4	573	7.7	53

All methods above improve the contact between ITO and CdTe, but have different issues that require fixing before they can be properly utilized (Table 3.VII). Some contacts need to increase transparency, consistency, or conductivity, all of which can be improved by testing different processing conditions. Two methods, etched CdTe:Cu and spincoated Te, have better longevity than current/light soaking (Table 3.VIII).

Table 3.VIII. Compiled table of device performance without current/light soaking over extended periods of time.

Device Longevity				
Interfacial Layer	PCE (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
Current/Light Soaked Control (immediate)	12.3	684	25.8	71
(1 day)	8.6	540	25.3	62
(1 week)	6.0	428	25.0	56
(~1 year)	3.5	350	22.0	45
Etched CdTe:Cu (immediate)	7.0	514	21.9	63
(1 day)	7.0	507	22.3	62
(1 week)	7.0	530	21.2	63
(~1 year)	4.1	543	15.5	49
Spincoated Te (immediate)	7.0	597	19.7	59
(1 day)	6.7	595	19.9	57
(1 week)	6.4	587	20.0	55
(~9 months)	5.4	543	19.8	50

Some of the degradation can be attributed to the contact between Al and Ag. Most notably, FF would decrease with an increase in series resistance.

We also found some interesting trends in devices that do require current/light soaking. Spincoated "ZnTe:Sb" can improve V_{oc} through the addition of extra Sb_2Te_3-N_2H_4 or current/light soaking (Table 3.IX). Spincoated layers of CdTe/A_2CdTe_2 improve as the alkali cation increases in size, presumably because of lower diffusivity (Table 3.IX).

Table 3.IX. Compiled table of device performance with current/light soaking.

Device With Current/Light Soaking				
Interfacial Layer	PCE (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)
Control (best)	12.3	684	25.8	71
Spincoated "ZnTe:Sb" (best)	6.4	732	16.1	54
CdTe/Na_2CdTe_2 (best)	8.5	629	19.7	69
CdTe/K_2CdTe_2 (best)	10.0	655	22.3	69
CdTe/Cs_2CdTe_2 (best)	12.0	674	24.4	73
CdTe/$(N_2H_5)_2CdTe_2$ (best)	12.7	726	24.6	71

3.8. Overall outlook of the various methods.

All of the methods we explored are compatible with one another. A combination of ZnTe:Cu, Te, and CdTe/$(N_2H_5)_2CdTe_2$ could be used to form a graded device stack. Such device design already has precedence.[4,11] Te and CdTe/$(N_2H_5)_2CdTe_2$ would act as a barrier, preventing Cu from diffusing into the CdTe absorber layer. All of these layers are transparent, making dual transparent electrodes possible (Figure 3.6). Through modeling, we have determined the most likely cause of rollover and device deficiencies as well as shown that dual TCO electrodes will not lower device performance substantially.

3.9. Acknowledgements.

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Hudson and Dr. Dmitriy Dolzhnikov performed A_2CdTe_2 ligand exchanges on CdTe NCs. Vadim Tanygin helped to establish basic protocols for device fabrication and testing. Dr. Joseph Luther helped to facilitate collaboration as well as explained SKPM data. Dmitri provided valuable insight into forming the manuscript as well as provide guidance for the overall course of research.

3.10. References.

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4. Solution-processed, ultrathin solar cells from trichlorocadmate-capped cadmium telluride nanocrystals: the multiple roles of trichlorocadmate ligands.

Solution-processed CdTe solar cells using CdTe nanocrystal ink may offer an economically viable route for large scale manufacturing. Here we design a new $CdCl_3^-$-capped CdTe nanocrystal ink by taking advantage of novel surface chemistry. In this ink, $CdCl_3^-$ ligands act as surface ligands, sintering promoters, and dopants. Our solution chemistry allows obtaining very thin continuous layers of high quality CdTe which is challenging for traditional vapor transport methods. Using benign solvents, in air, and without additional $CdCl_2$ treatment, we obtain a well-sintered CdTe absorber layer from the new ink, and demonstrate thin film solar cells with power conversion efficiency over 10%, a record efficiency for sub-400 nm thick CdTe absorber layer.

4.1. Progression of photovoltaics and nanocrystal ligand exchanges.

Over the past forty years, efforts to improve photovoltaics have taken crystalline silicon nearly to its theoretical limit.[1] Second-generation solar cells using direct gap semiconductors, such as CdTe, have developed to the stage of rivaling silicon.[2-3] Solution-processing offers an efficient and economically viable route to thin film CdTe solar cells. In particular, sintered CdTe thin film deposited from soluble CdTe nanocrystals (NCs) or "NC ink" has been proven effective as the absorber layer for CdTe solar cells.[4-8] Similar to the commercial CdTe photovoltaics made by vacuum-based techniques,[9] $CdCl_2$ treatment is critical for ensuring high efficiencies in solution-processed CdTe solar cells. It promotes the sintering of CdTe NCs into large grains and concurrently improves the carrier transport by doping the interfaces.[4-8] A new ink comprising both the active materials (CdTe NCs) and sintering promoters (e.g., $CdCl_2$) would be desirable for a facile solution-based fabrication of highly efficient CdTe solar cells.

Our design of the new ink containing sintering promoters was inspired by new developments in NC surface chemistry. During the past decade, the colloidal NC field has witnessed the rapid progress of new classes of inorganic surface ligands,[10] including the nucleophilic chalcogenides,[11] halides and pseudohalides,[12-15] and more elaborate multidentate chalcogenidometallates,[16-17] halometallates,[12,18-19] and (poly)oxometallates.[20-21] These inorganic surface ligands have significantly enhanced electronic coupling by decreasing interparticle distance, enabling efficient solution-processed field-effect-transistors (FET),[22-24] photodetectors,[22] and solar cells.[25] More interestingly, inorganic surface ligands can introduce new functionalities to NCs. For instance, we recently demonstrated several compositionally-matched molecular solders by controlling the surface chemistry of semiconductor NCs and microparticles.[26-28] These solders situated at the surface of grains, facilitating sintering and carrier transport across grain boundaries.

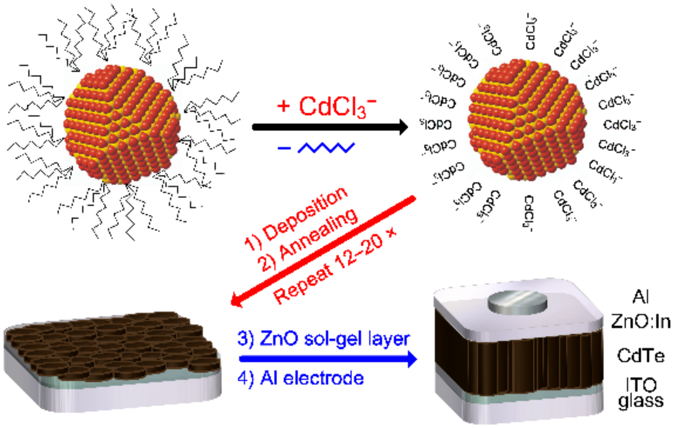

Figure 4.1. Solution-based fabrication of CdTe solar cells using the $CdCl_3^-$-capped CdTe nanocrystal ink.

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In this work, we harness chlorocadmate ($CdCl_3^-$) ligand chemistry to design a new CdTe NC ink for solution-processed solar cells (Figure 4.1). In this ink, $CdCl_3^-$ ligands play a dual role: i) to replace the organic ligands on CdTe NCs and afford a high solubility of NCs in a suitable solvent; ii) to promote CdTe grain growth. CdTe NCs in this new ink can efficiently sinter and grow into large grains. Moreover, chloride ions provide selective electronic doping of grain boundaries that helps to separate charge carriers in CdTe solar cells. The strategy of introducing new functionalities to NCs by the surface chemistry is anticipated to be generally employed to many other NC-based applications.

4.2. Experimental route to a new nanocrystal ink and its characterization.

4.2.1. Chemicals used to synthesize the new nanocrystal ink.

Cadmium oxide (CdO, 99.99+%, trace metal basis), ammonium chloride (NH_4Cl, 99.99%), cadmium chloride ($CdCl_2$, 99.99%, trace metal basis), pyridinium hydrochloride ($C_5H_5N{\cdot}HCl$, 98%), indium chloride ($InCl_3$, 99.999%), tellurium shot (Te, 99.999%), tributylphosphine (TBP, 97% with isomers), trioctylphosphine oxide (TOPO, 99%), oleic acid (OA, technical grade, 90%), oleylamine (OLA, 70%), tetradecylphosphonic acid (TDPA, 97%), 1-octadecene (ODE, technical grade, 90%), ethanolamine (99.5%, redistilled), hexamethylphosphoramide (HMPA, 99%), ethanol (≥99.5%, anhydrous), toluene (≥99.8%, anhydrous), hexane (95%, anhydrous), methanol (99.8%, anhydrous), acetonitrile (99.8%, anhydrous), pyridine (99.8%, anhydrous), propylene carbonate (99.7%, anhydrous), *N,N*-dimethylformamide (DMF, 99.8%, anhydrous), 1-propanol (1-PA, 99.7%, anhydrous), and 2-methoxyethanol (99.9%, anhydrous) were purchased from Aldrich. *N*-trioctylphosphine (TOP, 97%) was purchased from Strem. Acetone (certified ACS), methanol (certified ACS), and

2-propanol (IPA, certified ACS) were purchased from Fisher Scientific. 10 wt% TBP:Te was prepared by dissolving 10 g of Te shot in 90 g of TBP overnight in a N_2-filled glove box. ODE and OA were recrystallized by cooling the bottle in a chiller overnight at 12 and 18 °C, respectively, and decanted to remove impurities. Pyridine and 1-PA were distilled to remove low and high boiling point impurities. *N*-methylformamide (NMF, 99%, Alfa Aesar) and OLA were dried prior to use in glove box.

4.2.2. Cadmium telluride nanocrystal synthesis.

Monodisperse zinc-blende CdTe nanocrystals (NCs) capped with TDPA ligands were synthesized following the reported procedure.[29] In brief, CdO (128 mg), TDPA (570 mg), and ODE (39.3 g) were evacuated at 80 °C until equilibrated. Under dry N_2, the mixture was heated to 300 °C until all powders dissolved. At this temperature, a solution containing 2.5 g of 10 wt% TBP:Te, 2.5 g of TBP, and 15 g of ODE was swiftly injected. The reaction mixture immediately turned green and then orange within 30 s. Aliquots were taken at 1, 3, 4, and 5 min after injection and were quenched by adding toluene. The resulting CdTe NCs were purified using anhydrous solvents in the glove box. NCs were precipitated by a 1:1 mixture of anhydrous methanol and 1-propanol, and redispersed in toluene. Prior to the ligand exchange, NCs were precipitate with ethanol and redispersed in hexane.

Wurtzite CdTe NCs capped with oleate were synthesized with a modified method described in ref.[5,30] CdO (4.80 g), OA (42.4 g, recrystallized), and ODE (40.0 g, recrystallized) were loaded in a 500 mL three-necked flask and evacuated overnight to remove trace oxygen. Afterward, the flask was heated to 80 °C until the pressure equilibrated. Under dry N_2, the mixture was heated to 220 °C until the solution turned clear, indicating a completed reaction to form cadmium oleate ($Cd(OA)_2$). The flask was cooled and dried under vacuum at 110 °C to remove water generated by the reaction. Under dry N_2, the flask was heated to 270 °C, followed by the quick injection of 24 mL of 10 wt% TBP:Te. Immediately after the injection, the heating mantle was removed and the flask was quickly cooled to room temperature. The resulting CdTe NCs were purified using anhydrous solvents in the glove box. Ethanol was used as the non-solvent while toluene as the solvent. After several precipitation-redispersion cycles with ethanol/toluene, the purified NCs were dissolved in hexane at a concentration of ~80 mg/mL.

Wurtzite CdSe NCs capped with OA were synthesized using $Cd(OA)_2$ as the Cd precursor. In brief, 1.2 g of TOPO, 2.25 mL of 1.0 M $Cd(OA)_2$ solution in OA, and 12 mL of ODE were loaded in a 100 mL three-necked flask and dried under vacuum at 70 °C for 1 h. Afterward, the solution was heated to 300 °C under N_2. A stock solution containing 4 mL of 1.0 M TOPSe solution in TOP and 3 mL of OLA was swiftly injected at 300 °C. The mixture was kept at 280 °C for 2–3 min and quickly cooled to room temperature. The CdSe NCs can be isolated by adding ethanol to the crude solution followed by centrifugation. CdSe NC precipitates can redisperse in nonpolar solvents (e.g., hexane). The washing with ethanol/hexane as non-solvent/solvent was repeated several cycles to remove excess organic ligands. Finally, the purified CdSe NCs were dissolved in hexane.

4.2.3. Trichlorocadmate and pyridine exchanges on cadmium telluride nanocrystals.

To prepare a soluble CdTe NC ink for fabricating CdTe thin films using the “standard” or “additive” approach, CdTe NC solution in toluene was precipitated with ethanol and redispersed in anhydrous pyridine at a concentration of ~80 mg/mL. The solution of CdTe NCs in pyridine was stirred under N_2 overnight on a hotplate set to 100 °C, followed by precipitation using hexane. The CdTe NC precipitates were redispersed in fresh pyridine to prepare the “pyridine-exchanged” CdTe NC ink for the “standard” or “additive”.

Chlorocadmates ($CdCl_3^-$) with NH_4^+ or $C_5H_5NH^+$ cations were synthesized by mixing equimolar amount of $CdCl_2$ and NH_4Cl or $C_5H_5N{\cdot}HCl$ in NMF (0.1 M). In a typical ligand exchange, 3 mL of oleate-capped CdTe NC solution in hexane (~30 mg/mL) was mixed with 3 mL of $CdCl_3^-$ solution in NMF (0.1 M). Under vigorous stirring, NCs gradually transferred from hexane to NMF. Typically, it took up to several hours until a complete phase transfer, resulting in a colorless hexane phase. The time required for ligand exchange was strongly dependent on the concentration of NCs, and also affected by the cations of chlorocadmates. A much shorter time (within 15 min) is required for CdTe NCs with a lower concentration (5 mg/mL). The bottom phase containing CdTe NCs was then rinsed with fresh hexane three times. In detail, 3 mL of fresh hexane was mixed with the solution of $CdCl_3^-$-capped CdTe NCs in NMF, forming a two-phase mixture. This mixture was vigorously stirred for about 20 min. During this process, residual organic ligands and related species soluble in the nonpolar hexane phase were removed from the NC solution in NMF. The hexane layer was then discarded and replaced with fresh hexane. After a triple wash with hexane, a mixture of toluene (1 mL) and HMPA (0.5 mL) was added, leading to the flocculation of NC solution. The NC precipitates were collected by centrifugation, and re-dispersed in 1 mL of propylene carbonate or pyridine. The ligand exchange procedure can be scaled up to produce >1 g of $CdCl_3^-$-capped CdTe NCs in a single batch. The solution of $CdCl_3^-$-capped CdTe NCs in pyridine was vigorously stirred for ~1 h in air, followed by centrifugation to remove the insoluble part. The concentration of the colloidally stable solution (the "$CdCl_3^-$-capped CdTe NC ink") can be as high as 150 mg/mL. In pyridine, $CdCl_3^-$-capped NCs with $C_5H_5NH^+$ cations showed a slightly higher solubility than those with NH_4^+, presumably due to the compatibility of the cation and the solvent.

4.2.4. Characterization of nanocrystals and the subsequent material.

Transmission electron microscopy (TEM) images of NCs were obtained using a 300 kV FEI Tecnai F30 microscope. The optical absorption spectra of NC solutions were collected using a Cary 5000 UV-Vis-NIR spectrophotometer in the transmission mode. To investigate the evolution of size and excitonic features of $CdCl_3^-$-capped CdSe NCs, thin films were prepared by drop-casting NC solution in NMF on quartz substrates, followed by dried under vaccum to remove the solvent. The dried $CdCl_3^-$-capped CdSe NC thin films were annealed at various temperatures on a hot-plate in a N_2-filled glove box. The absorption spectra of thin films were measured in the transmission mode. Fourier-transform infrared (FTIR) spectra were acquired in the transmission mode using a Nicolet Nexus-670 FTIR spectrometer. Samples for FTIR measurements were prepared by drop casting concentrated NC dispersions on KBr crystal substrates (International Crystal Laboratories) and were then dried under vacuum to remove solvent molecules. Additional annealing at 200 °C under vacuum was applied to the $CdCl_3^-$-capped NC samples to completely remove any residual solvents. IR absorbance was normalized to the weight of absorbing material deposited per unit area of the substrate. To quantitatively compare IR spectra, we applied standard background subtraction and baseline correction routines. Scanning electron microscopy (SEM) images of sintered CdTe thin films and the complete CdTe solar cell devices were acquired on FEI NanoSEM Nova 200 (top-view), FEI NanoSEM Nova 630 and Zeiss-Merlin (cross-sectional), respectively. For top-view SEM, single-layer CdTe thin films were deposited on silicon substrate from the new $CdCl_3^-$-capped CdTe NC ink (annealed at 350 °C for 20 s). The same CdTe thin films were used for wide angle powder X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) measurements. The XRD patterns of CdTe thin films made from organically capped CdTe NCs and the new ink were collected using a Bruker D8 diffractometer with a Cu K_α X-ray source operating at 40 kV and 40 mA. In-situ XRD measurements were carried out by ramping the temperature from 25 to 600 °C (3 °C/min) with frames taken every 195 sec. The thin film samples were enclosed in a O-ring sealed dome with a plastic cap and a temperature-controllable metallic bottom. The dome was evacuated and re-filled with N_2 several cycles to remove residual air or moisture prior to the measurement. Afterward, the dome was kept under vacuum during the in-situ measurement. The samples were annealed by the temperature-controllable bottom part of the dome during the measurement. The source and detector of the diffractometer were set to 19° with respect to horizontal. A 2D intensity color map was made by compiling the frames using a homemade Matlab software. XPS analysis on sintered CdTe thin films made from "standard", "additive", and the new $CdCl_3^-$-capped CdTe NC ink was performed on a Kratos AXIS Nova spectrometer using a monochromatic Al K_α source (hν = 1486.6 eV). The Al anode was powered at 10 kV and 15 mA. Instrument base pressure was 1×10^{-9} Torr. High-resolution spectra in Cd 3d, Te 3d, C 1s, and Cl 2p regions were collected using an analysis area of 0.3×0.7 mm^2 and 20 eV pass energy. All spectra were background subtracted using XPS subtraction software in Origin. Te and Cd spectra were subtracted using a Tougaard algorithm while C and Cl used a Shirley algorithm. The XPS intensities for all elements were normalized to the area under the Cd 3d curves for proper comparison. Zeta-potential (ζ-potential) data were collected using a Zetasizer Nano-ZS (Malvern Instruments, UK).

4.2.5. Sintered cadmium telluride nanocrystal photovoltaic fabrication.

In the "standard' approach, the CdTe absorber layer was spin-coated from pyridine-exchanged CdTe NC ink through a layer-by-layer deposition approach, together with interlayer chemical ($CdCl_2$) and thermal treatment (350 °C, 20 s). In detail, 25 mm×25 mm indium tin oxide (ITO)-coated glass substrates (Thin Film Devices Inc) were cleaned by sequential sonication in deionized water (DI) and Alconox detergent, DI, acetone, IPA, and DI. Afterward, the substrates were dried under N_2, and hydrophilized for 10 min using a Harrick PDC-001 Extended Plasma Cleaner. The pyridine-exchanged CdTe NC solution was precipitated by hexane and dissolved in a 1:1 mixture of pyridine and 1-PA at the desired concentration. The solution was sonicated for 10 min and filtered through a 0.2 μm PTFE syringe filter. The filtered CdTe NC solution was spin-coated onto an ITO substrate at 800 rpm for 30 s followed by 2000 rpm for 10 s, dried at 150 °C for 2 min, and cooled in air. For the $CdCl_2$ treatment, the spin-coated CdTe layer was dipped in a saturated $CdCl_2$ bath in methanol for 15 s, thoroughly rinsed with IPA and dried under N_2 flow. The substrate was annealed at 350 °C for 20 s and cooled in air. The whole process (spin-coating, $CdCl_2$ treatment, thermal treatment) was repeated multiple times (12–20) until the desired thickness was achieved. Using this approach, devices with ~400 or ~550 nm-thick CdTe active layers were fabricated by spin-coating different layers of CdTe NC ink.

The ZnO layer was deposited on top of CdTe by spin-coating 300 μL of ZnO sol-gel at 3000 rpm for 30 s, followed by annealing at 300 °C for 2 min. The ZnO sol-gel was prepared by sonicating a mixture of 1.50 g of zinc acetate dihydrate, 15 mL of 2-methoxyethanol, 420 μL of ethanolamine, and 15–45 mg of $InCl_3$ for 1 h, and subsequently stirred overnight.

After the deposition of ZnO layer, the substrates were transferred into a glove box and kept under high vacuum overnight. Top Al contacts (100 nm) were deposited by thermal evaporation through a homemade mask, featured by evenly distributed 8 mm^2 holes. Ag (100 nm) was deposited on top of Al to increase device longevity. Three sides of the device stack were scratched off to expose the ITO. Electrical contact was established using colloidal Ag paint (Ted Pella Inc).For XPS studies on thin films made from the “standard” approach, a single layer of CdTe was deposited on ITO or silicon substrate, followed by $CdCl_2$ treatment and annealing.

In the "additive" approach, about 5 wt% of $CdCl_2$ (with respect to the amount of CdTe NCs) was added to the pyridine-exchanged CdTe NC ink. The mixture was used as the soluble precursor for CdTe layers. Solar cell device fabrication was performed in a similar manner with the "standard" approach without the interlayer $CdCl_2$ treatment. For XPS study, a single layer of CdTe was deposited on ITO from the mixture of $CdCl_2$ and pyridine-exchanged CdTe NC ink, followed by annealing at 350 °C for 20 s.

A similar, but $CdCl_2$ treatment-free approach was adopted in the fabrication of CdTe adsorber layer from the designed $CdCl_3^-$-capped CdTe NCs ink. In brief, the $CdCl_3^-$-capped CdTe NC solution in pyridine was diluted with 1-propanol in a 1:1 volume ratio, forming an ink of about 40 mg/mL. Layers of CdTe were spin-coated on an ITO substrate with interlayer thermal treatment (350 °C, 20 s) for CdTe grain growth. For XRD, top-view SEM, and XPS studies on CdTe thin films from the new ink, a single layer of CdTe was deposited on ITO or silicon substrate, followed by annealing.

4.2.6. Cadmium telluride solar cell characterization.

Devices were tested under the illumination of a Xe lamp with a AM 1.5G filter (Newport 67005) and calibrated with a Si photodiode with a KG5 filter (Hamamatsu Inc, S1787-04). The illumination area was controlled by a self-aligning stainless steel aperture mask with evenly distributed, nominally 6 mm^2 circular holes (5.94 mm^2 measured). *JV* characteristics were acquired using a Keithley 2400 sourcemeter controlled by a Labview interface. To mitigate heating during measurements, the perimeter of the cell was in direct contact to an Al heat sink. The instruments were controlled and data collected using a homemade Labview program. Current/Light soaking was done by applying 2–3 V (forward bias) to the device under illumination for 5 min (7 min for devices made from the "standard" approach with a

~550 nm-thick CdTe layer). Typically, this generated a current density of ~2.5 A cm^{-2}. The current was monitored carefully to not exceed a 3 A cm^{-2}, as current densities greater than this generally caused performance degradation. Holding the devices in reverse bias generally caused a transient decrease in performance (due to reduced V_{OC}). External quantum efficiency (EQE) and interal quantum efficiency (IQE) measurements were taken using Oriel IQE-200 with a step of 10 nm for the wavelength. Capacitance-voltage (Mott-Schottky) data were acquired using a Gamry Reference 600 potentiostat. Data were acquired using a frequency of 500 Hz with an amplitude and step size of 5 and 10 mV, respectively. To compare performance of devices made from the "standard" approach and the new $CdCl_3^-$-capped CdTe NC ink, the same batch of oleate-capped CdTe NCs were used. Pyridine-exchange and ligand exchange with $CdCl_3^-$ were carried out on NC for the "standard" and the new ink, respectively. Solar cells with ~400 and ~600 nm CdTe active layers were fabricated by using both approaches with all other procedures (e.g., treatment of ITO substrates, the deposition of ZnO and Al/Ag layers) identical.

4.2.7. Cadmium selenide field effect transistor fabrication and characterization.

Prime grade, n-type arsenic doped Si wafers with 100 nm-thick SiO2 gate dielectrics (<0.005 Ω cm, NamKang High-Tech) were used as gate substrates. The substrates were cleaned by piranha treatment followed by multiple rinses with DI water before use. Solutions of $CdCl_3^-$-capped CdSe NCs (~ 70 mg/ml in NMF) were spin-coated on the cleaned substrates at 600 rpm for 6 s, followed by 2000 rpm for 60 s. A 500 W infrared lamp was used to maintain the temperature of solutions and substrates at ~70 °C. The resulting 30–40 nm-thick NC films were annealed at 100 °C for 1 h to evaporate residual solvents, and then annealed at 200, 250, 300, or 350 °C for 30 min. 100 nm-thick Al source/drain electrodes were thermally evaporated through a shadow mask to complete a top-contact, bottom-gate field effect transistor (FET) structure (channel width W: 1500 μm and channel length L = 125 μm). All fabrication steps except substrate cleaning were performed in a N_2-filled glove box. We also tried the ligand exchange of CdSe NCs with NH_4CdCl_3 and deposition of the FET channel in air. In this case, the spin-coating of $CdCl_3^-$-capped CdSe NCs on gate substrates was performed in air, followed by the thermal annealing at 300 °C for 30 min. The source/drain electrodes were evaporated in a N_2-filled glove box.

FET devices were measured using a semiconductor analyzer (Agilent B1500A) in a N_2-filled glovebox. The linear regime FET mobility was calculated by fitting the experimental data to the following Equation 4.1.

$$\mu = \frac{L}{W\, C_i\, V_{DS}} \frac{\partial\, I_{DS}}{\partial\, V_G} \tag{4.1}$$

where C_i, V_{DS}, I_{DS}, and V_G are the capacitance per unit area, drain-source voltage, drain current, and gate voltage, respectively. The equation applies to the linear regime of transistor operation.

4.3. Understanding the trichlorocadmate ligand exchange.

Preparing the new ink involved the exchange of insulating, long hydrocarbon ligands with $CdCl_3^-$ (Figure 4.1). Spherical CdTe NCs (Figure 3.2c) were synthesized using tetradecylphosphonic acid (TDPA) according to reported methods.[29] For ligand exchange, we combined CdTe NCs dissolved in hexane with a solution of NH_4CdCl_3 in *N*-methylformamide (NMF). These two immiscible phases were stirred until CdTe NCs transferred to NMF and formed a stable colloid (Figure 4.2a). After purification, the ligand-exchanged CdTe NCs can redisperse in several solvents, including NMF, propylene carbonate, and pyridine. The deployment of NH_4CdCl_3 as surface ligands for colloidal NCs was first reported by Dirin et al.[18]

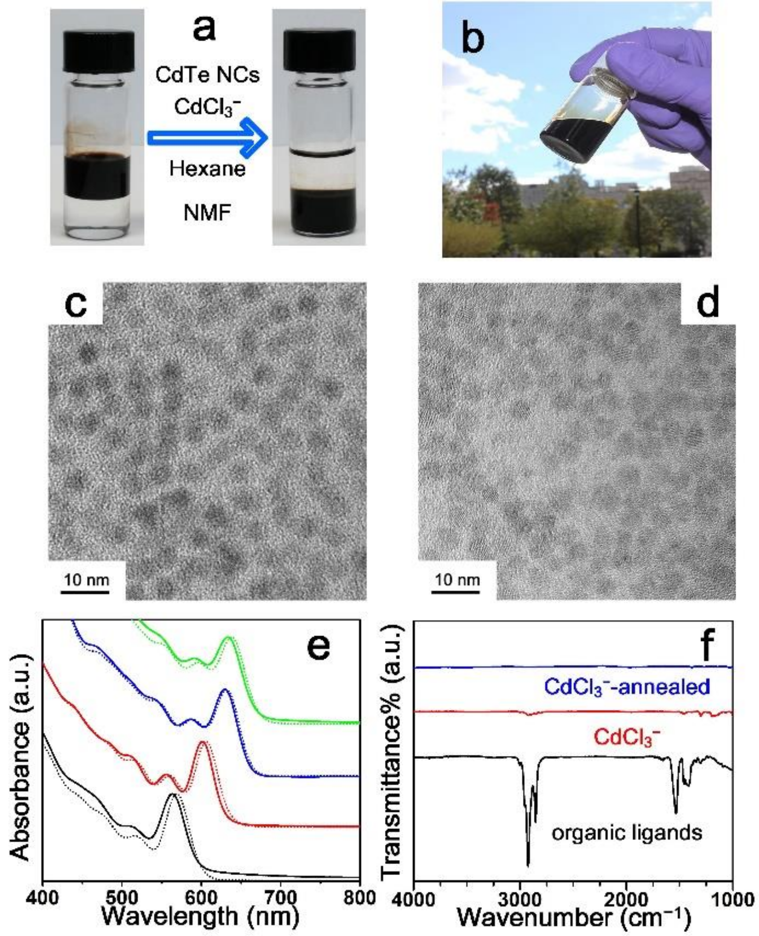

Figure 4.2. (a) A photograph showing the black-colored CdTe nanocrystals transferring from hexane to *N*-methylformamide (NMF) in the presence of $CdCl_3^-$ ligands. (b) A photograph of a concentrated $CdCl_3^-$-capped CdTe nanocrystal ink. (c,d) TEM images of CdTe nanocrystals capped with tetradecylphosphonic acid and $CdCl_3^-$ (NH4CdCl3) ligands, respectively. (e) UV-visible spectra of CdTe nanocrystals with various sizes capped with tetradecylphosphonic acid (dotted lines) and $CdCl_3^-$ ligands (solid lines). (f) FTIR spectra of CdTe nanocrystals capped with native oleate ligands and $CdCl_3^-$ through a large-scale ligand exchange.

NH_4CdCl_3-capped NCs were colloidally stable as $CdCl_3^-$ (and other anions generated by self-ionization) bound to the NC surface and provided electrostatic repulsion to overpower the interparticle van der Waals attractive force. The binding of negatively charged $CdCl_3^-$ anions to NC surface was confirmed by the negative zeta-potential (−34 mV, Figure 4.3) of NH_4CdCl_3-capped CdTe NCs in propylene carbonate.

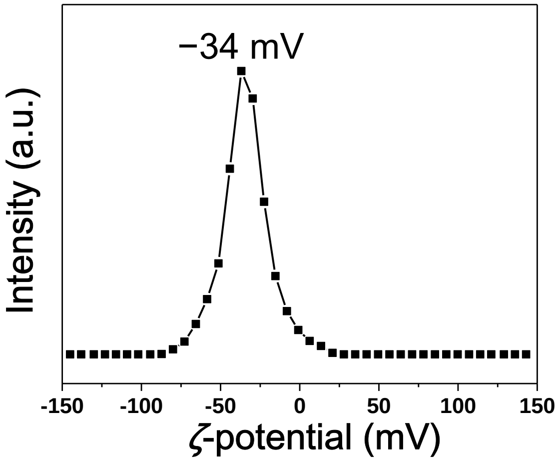

Figure 4.3. Zeta-potential of CdTe NCs capped with NH_4CdCl_3 ligands in propylene carbonate.

Transmission electron microscopy (TEM) images (Figure 4.2d) indicated that NCs retained their size and morphology. The integrity of CdTe NC cores after ligand exchange was also demonstrated by the optical absorption spectra. The absorption spectra (Figure 4.2e) of $CdCl_3^-$-capped CdTe NCs of various sizes resembled those of TDPA-capped ones. The ligand exchange procedure using NH_4CdCl_3 can be extended to CdTe NCs with other organic surfactants or morphologies (e.g., oleate-capped CdTe tetrapods) and, more importantly, performed on a large scale. An ink containing several grams of $CdCl_3^-$-capped CdTe NCs can be made in a single batch (Figure 4.2b). The completeness of ligand exchange on such a large scale was monitored by Fourier transform infrared (FTIR) spectroscopy. The vibrational peaks observed in FTIR (Figure 4.2f) arising from native organic ligands (e.g., 2800–3000 cm^{-1} for C–H stretching mode, 1300–1500 cm^{-1} for C–H bending) were drastically suppressed in NCs with $CdCl_3^-$ ligands. The weak IR features for $CdCl_3^-$-capped CdTe NCs could be assigned to solvent residue and counterions, as they disappeared after mild annealing (200 °C under vacuum). Besides NH_4CdCl_3, $CdCl_3^-$ moieties with other cations can also behave as ligands for CdTe NCs. For instance, reacting an equimolar mixture of $CdCl_2$ and pyridinium hydrochloride in NMF resulted in soluble species containing $CdCl_3^-$ and $C_5H_5NH^+$. CdTe NCs capped with this compound (further referred to as $pyrHCdCl_3$) showed similar UV-visible absorption features to those capped with NH_4CdCl_3 (Figure 4.4). Moreover, $pyrHCdCl_3$ allowed a higher solubility (up to 150 mg/mL) of CdTe NCs in low boiling point solvents (pyridine, its mixture with alcohols, and nearly pure alcohols with several percent pyridine), which was crucial for the solution-based fabrication of high quality CdTe thin films.

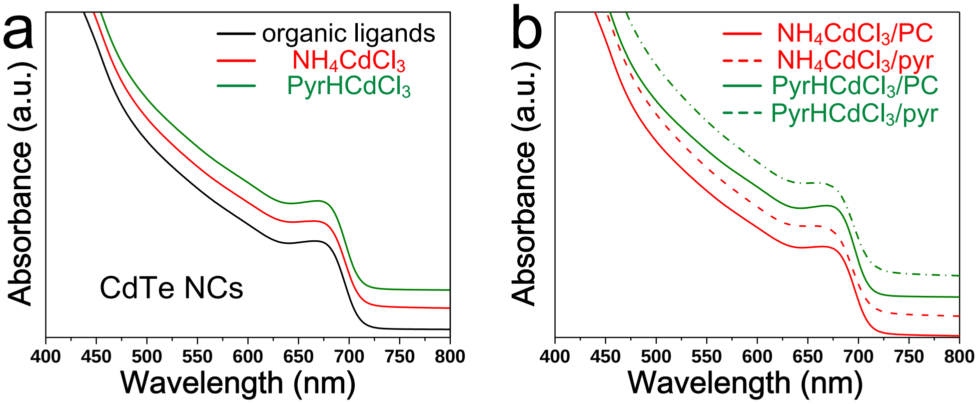

Figure 4.4. (a) UV-visible spectra of CdTe NCs capped with oleate (in toluene, black curve) and $CdCl_3^-$ ligands (in propylene carbonate). (b) Comparsion of UV-visible spectra of $CdCl_3^-$-capped CdTe NCs in propylene carbonate (PC) and pyridine (pyr).

4.4. Probing grain growth of nanocrystals with various capping ligands.

In this new ink, the surface-bound $CdCl_3^-$ molecules play a vital role as the grain growth promoter of CdTe NCs. CdTe NCs before and after $CdCl_3^-$ ligand exchange showed significantly different sintering behavior (Figure 4.5). Broad peaks (centered at ~39°, ~42.5°, and 46.5°) with low intensities (as indicated by the blue color, Figure 4.5e) were observed in the case of as-synthesized CdTe NCs, corresponding to small CdTe grains (diameter about 5 nm). The native organic ligands inhibited the sintering of NCs, even at high temperatures, as indicated by the minor changes in intensities and widths of XRD peaks (Figure 4.5e). Exchanging native oleate ligands for pyridine did not result in a significant promotion of CdTe grain growth upon the heat treatment (Figure 4.5e).

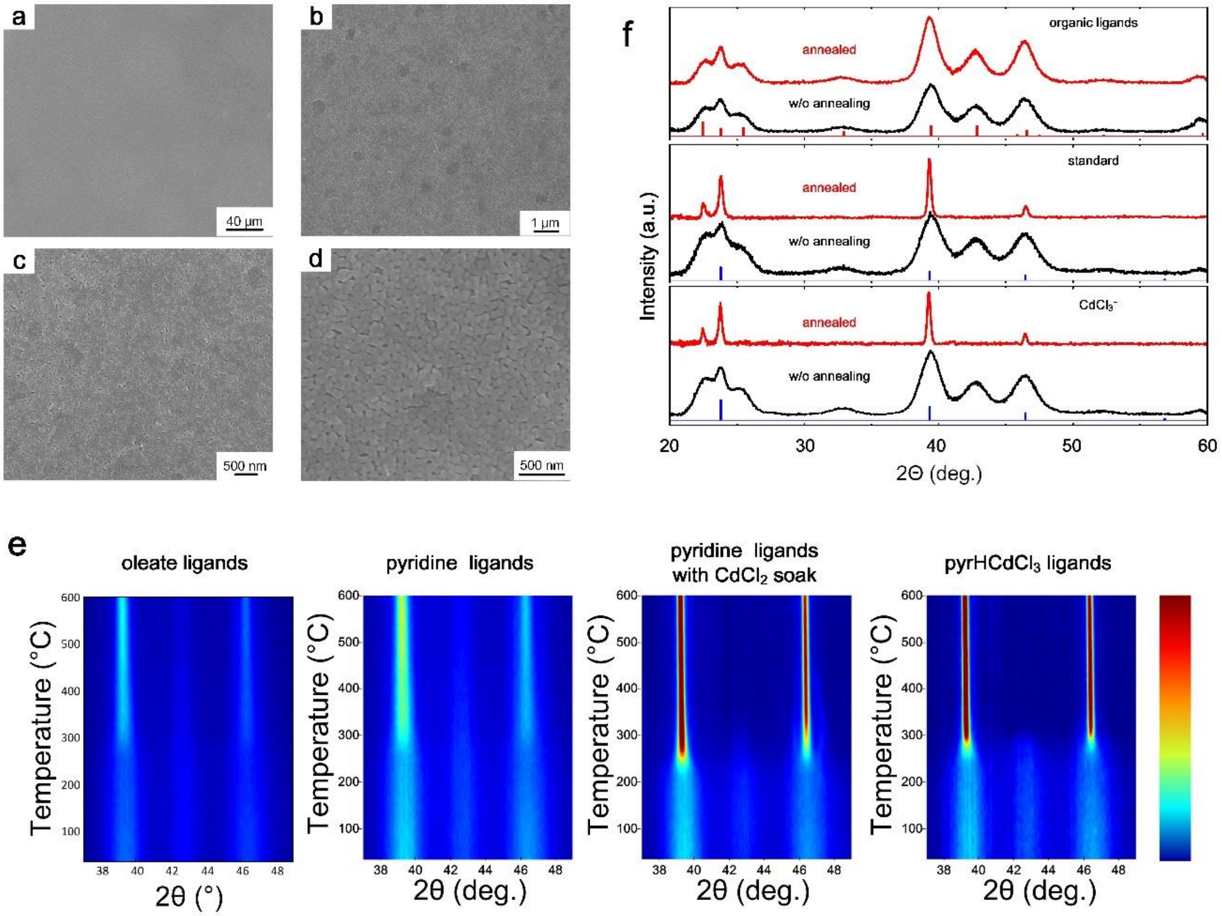

Figure 4.5. (a–d) Top-view SEM images of a single-layer CdTe thin film made from $CdCl_3^-$-capped CdTe NC ink. (e) In-situ and (f) Ex-situ XRD patterns of single-layer CdTe thin films made from as-synthesized oleate-capped CdTe NCs, pyridine-exchanged NCs, pyridine-exchanged NCs soaked in saturated methanolic $CdCl_2$ solution using "standard" approach, and $CdCl_3^-$-capped CdTe NCs. The Ex-situ XRD patterns of thin films without (w/o) annealing and annealed at 350 °C for 20 s are compared. The vertical lines in (f) show the corresponding X-ray diffractions of bulk CdTe in wurtzite (red in the top panel) and zinc-blende (blue in the bottom panel) phase, respectively. The peak at 22.4° for the annealed "standard" and new ink-based thin films has been suspected to be TeO_2 formed during annealing in the air.[7,30]

In contrast, the grain growth in $CdCl_3^-$-capped CdTe NCs was considerably enhanced, as evidenced by the high intensities (red color) and narrowing of the XRD peaks starting from ~250 °C (Figure 4.5e). Concomitantly, a characteristic peak for wurtzite phase (~42.5°)

disappeared, indicating a complete transition to zinc-blende phase. As further evidence of grain growth, scanning electron microscopy (SEM) images of an annealed, single-layer CdTe film deposited from $CdCl_3^-$-capped CdTe NC ink revealed a uniform film of well-connected, sintered CdTe grains (Figures 4.5a-d). Cross-sectional SEM (Figure 4.8a) of the complete CdTe device also showed a CdTe layer composed of sintered grains comparable in size to the thickness of the entire absorber film.

4.5. Cadmium telluride solar cells from the new nanocrystal ink.

4.5.1. Evaluating alternative methods with x-ray photoelectron spectroscopy.

Prior to the design of $CdCl_3^-$-capped CdTe NC ink, we attempted to use CdTe NCs with several other inorganic surface ligands, including Cl^-, Te^{2-}, and $CdTe_2^{2-}$.[11-13,27] The simple halide, Cl^-, failed to afford highly concentrated, stable colloidal solution of CdTe NCs (solubility < 30 mg/mL), which is a prerequisite for solution-processed solar cells. CdTe NCs capped with Te^{2-} and $CdTe_2^{2-}$ sintered after annealing without $CdCl_2$ treatment, but had been too air sensitive. Besides, adding $CdCl_2$ to pyridine-exchanged CdTe NCs (or "additive approach") was unable to remove the organic ligands and led to poor device performance (Figures 4.6 and 4.7). For proper comparison of concentrations of elements in single-layer CdTe thin films made from different approaches, the XPS intensities for Te 3d, C 1s, and Cl 2p were normalized by the area under Cd 3d curves in Figure 3.6a. The normalized Cd 3d curves for thin films made from the "standard" approach and new $CdCl_3^-$-capped CdTe NC ink were similar, while those for the sample made from "additive" approach showed shoulder peaks at higher binding energies. These components should be attributed to residual $CdCl_2$ since a large amount of $CdCl_2$ (5 wt% with respect to CdTe) was introduced to the pyridine-exchange CdTe NCs for the "additive" approach.

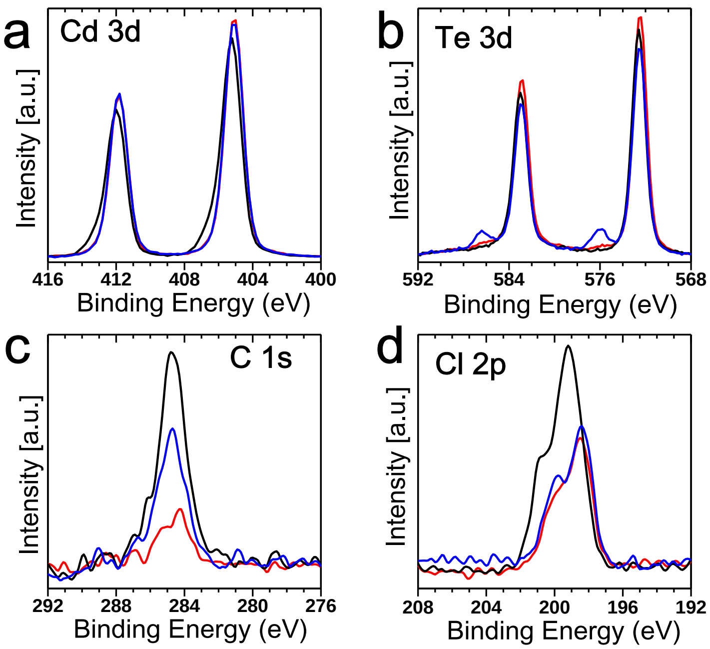

Figure 4.6. XPS spectra comparing sintered single-layer CdTe thin films made from "standard" (red), "additive" (black), and the new $CdCl_3^-$-capped CdTe nanocrystal ink (blue) in (a) Cd 3d, (b) Te 3d, (c) C 1s, and (d) Cl 2p regions.

As expected, similar intensities were observed in Te 3d spectra for different samples (Figure 4.6b). Thin film made from the new ink showed two peaks at higher binding energies (~585 and ~576 eV for Te $3d_{3/2}$ and $3d_{5/2}$, respectively), probably due to the formation of tellurium oxides at the surface. Importantly, thin films made from the "standard" approach and the new ink showed much reduced C 1s intensities compared to the "additive" sample (Figure 4.6c). This reduction in carbon content, or the amount of residual organic ligands, is critical to achieve efficient charge separation and transport, which govern the overall power conversion efficiency (PCE). As a consequence, solar cells made from the "additive" approach, with a significantly higher amount of residual organic ligands, suffered from poor device performance (Figure 4.7).

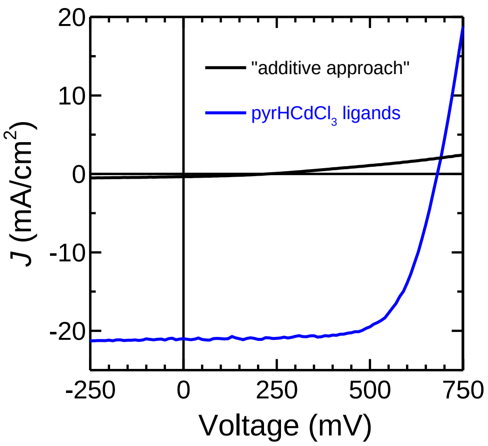

Figure 4.7. *JV* curves for CdTe solar cells made with "additive" approach (black), and the new $CdCl_3^-$-capped CdTe NC ink (blue, layer thickness <400 nm) approach, respectively. All devices are under AM 1.5G illumination.

Figure 4.6d confirms the existence of Cl in all samples. According to previous research, the CdTe sintering/recrystallization occurs with the formation of Te–Cl compounds ($TeCl_2$ or $TeCl_4$) in a liquid or gas phase, which enhance the mobility of nearby Cd and Te atoms, resulting in well-sintered CdTe grains.[8,31] In the new ink, the surface $CdCl_3^-$ ligands provide adequate Cl^- for CdTe NC sintering.

4.5.2. Solar cell efficiencies of the standard approach and the new nanocrystal ink.

In comparison, the robust $CdCl_3^-$-capped CdTe NC ink in a mixture of pyridine and 1-propanol can be processed in air and produced high quality CdTe layers using a layer-by-layer approach without additional $CdCl_2$ treatment. By using a device architecture outlined in Figure 4.8a and current/light soaking,[6] we achieved solar cells with ~350 nm thick CdTe absorber showing PCE 10.3% with short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF) of ~21 mA/cm^2, ~690 mV, and ~70%, respectively (Figure 4.8b and Table 4.I). The average values achieved were ~9%, ~20 mA/cm^2, ~670 mV, and ~68% for PCE, J_{SC}, V_{OC}, and FF, respectively (Table 4.I).

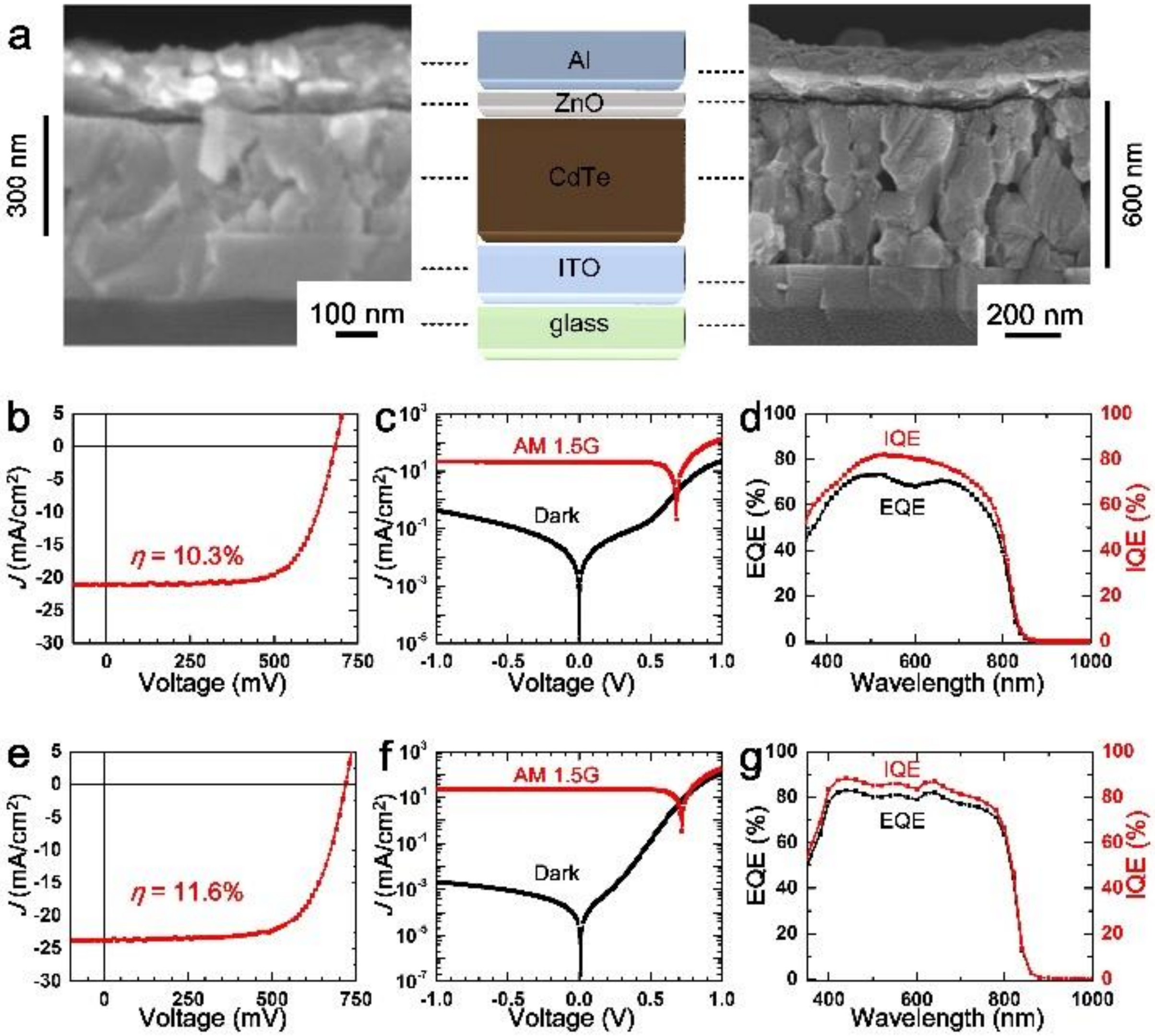

Figure 4.8. (a) Schematic and cross-sectional SEM image of complete CdTe solar cell devices made from $CdCl_3^-$-capped CdTe nanocrystal ink with (left) ~350 nm and (right) 600 nm-thick CdTe layers. (b–g) Device characteristics for CdTe solar cells with (b–d) ~350 nm and (e–g) 600 nm-thick CdTe active layers, respectively. (b,e) Current density-voltage (JV) curve under AM 1.5G illumination. (c,f) Light and dark JV curves and (d,g) External quantum efficiency (EQE) and internal quantum efficiency (IQE) spectra for the solar cells shown as black and red curves, respectively.

Table 4.I. Summary of performance of CdTe solar cells made from the "standard" approach and the new $CdCl_3^-$-capped CdTe NC ink (spin- or spray-coated) under AM 1.5G illumination.

Ink		**Deposition**	**Thickness (nm)**	**PCE (%)**	**V_{OC} (mV)**	**J_{SC} (mA/cm^2)**	**FF (%)**
New ink	Best	Spin-coated	~350	**10.3**	**690**	**21.4**	**70**
	Typical			9.0	670	20.0	68
New ink	Best	Spin-coated	~600	**11.6**	**718**	**23.7**	**68**
	Typical			10.0	680	22.0	67
New ink	Best	Spray-coated	~350	**8.8**	**650**	**21.4**	**63**
	Typical			8.0	650	20.0	60
"Standard"	Best	Spin-coated	~400	**9.6**	**598**	**22.2**	**72**
	Typical			8.0	550	21.0	
"Standard"	Best	Spin-coated	~550	**12.3**	**684**	**25.8**	**71**
	Typical			11	650	24.5	69

The photocurrent collected on each single CdTe solar cell device (area: 8 mm^2) was generated by an incident light exposed to an area of 6 mm^2 using an aperture mask. The external quantum efficiency (EQE) spectrum (Figure 4.8d) matched well with the measured J_{SC}. Internal quantum efficiency (IQE) (Figure 4.8d) was about 10% higher compared to EQE values, consistent with an estimate for light reflection at the air/glass interface. These reasonably high PCE values compared favorably with devices with very thin CdTe layers. Traditional CdTe solar cells use several micron thick CdTe layers, which poses obvious concerns given Te scarcity and Cd toxicity issues. Solution deposition can be easily scaled to different film thickness as shown in Figure 4.8a by simply adjusting the concentration of NC ink and the number of deposited layers. For example, the solar cells with ~600 nm thick CdTe layer showed PCE 11.6% due to improvements in both J_{SC} (23.7 mA/cm^2) and V_{OC} (718 mV) with FF 68% (Figures 4.8e-g and Table 4.I). Extensive studies of sputtered ultrathin CdTe solar cells demonstrated optimized 11% PCE for 0.5 µm CdTe layer and 8% record efficiency for devices with 0.25 µm CdTe due to shunting and incomplete light absorption.[32] Switching from gas-phase to solution deposition clearly helps to improve the uniformity of ultrathin CdTe layer (Figure 4.8a) resulting in 10% PCE for devices with sub-400 nm absorber. We anticipate the room for further improvements through the optimization of device stack and deposition conditions, e.g., by annealing the CdTe layers not in air but under controlled atmosphere.

In a series of control experiments, we compared performance of CdTe solar cells made of CdTe NCs capped with the $pyrHCdCl_3$ surface ligands and of the same batch of NCs but capped with pyridine. In the latter case, each spin-coated NC layer was soaked in a saturated solution of $CdCl_2$ in methanol before annealing at 350 °C ("standard approach").[6,33] We noted that at comparable thickness of CdTe absorber layers, the solar cells made with $pyrHCdCl_3$ surface ligands showed comparable or higher PCE values primarily originated from a significant increase in V_{OC} (Table 4.I). This difference in V_{OC} can be ascribed to a better passivation of grain boundaries and reduced Shockley-Read-Hall recombination velocity in the CdTe layer.[6]

The ability to integrate the grain growth promoter in form of the surface ligands for CdTe NCs made our new ink compatible with high throughput deposition methods, such as spray-coating or doctor blading. In preliminary tests for spray-coated solar cells, we achieved PCE (8–9%, Table 4.I) comparable to spin-coated devices, using $CdCl_3^-$-capped CdTe NC ink in methanol with a small amount of pyridine. This suggested the possibility of high-throughput, roll-to-roll large area deposition of CdTe layers by using the new ink on various substrates.

4.6. Adaptation of halometalate ligand chemistry to other materials.

4.6.1. Cadmium selenide field effect transistors.

Inspired by the successful design of $CdCl_3^-$-capped CdTe NC ink, we envisage a wide variety of potential applications of hallometallate-capped II–VI NCs and their alloys. As a preliminary step, we utilized $CdCl_3^-$-capped CdSe NCs to fabricate FET devices. Similar to the case of CdTe, CdSe NCs can disperse in NMF with NH_4CdCl_3 ligands without notable changes in the crystal size (Figure 4.9). $CdCl_3^-$ ligands promoted the grain growth of NCs with respect to other ligands, such as I^-. The sintered CdSe nanograins (~20 nm) showed decent electron mobility up to ~30 cm^2/Vs, depending on the annealing temperature, estimated from the FET transfer characteristics (Figure 4.10). More interestingly, the air-stable $CdCl_3^-$ ligands allowed the ligand exchange process and FET channel fabrication, for the first time, to be performed in air, resulting in CdSe FETs with preliminary mobilities of ~2–3 $cm^2/V{\cdot}s$.

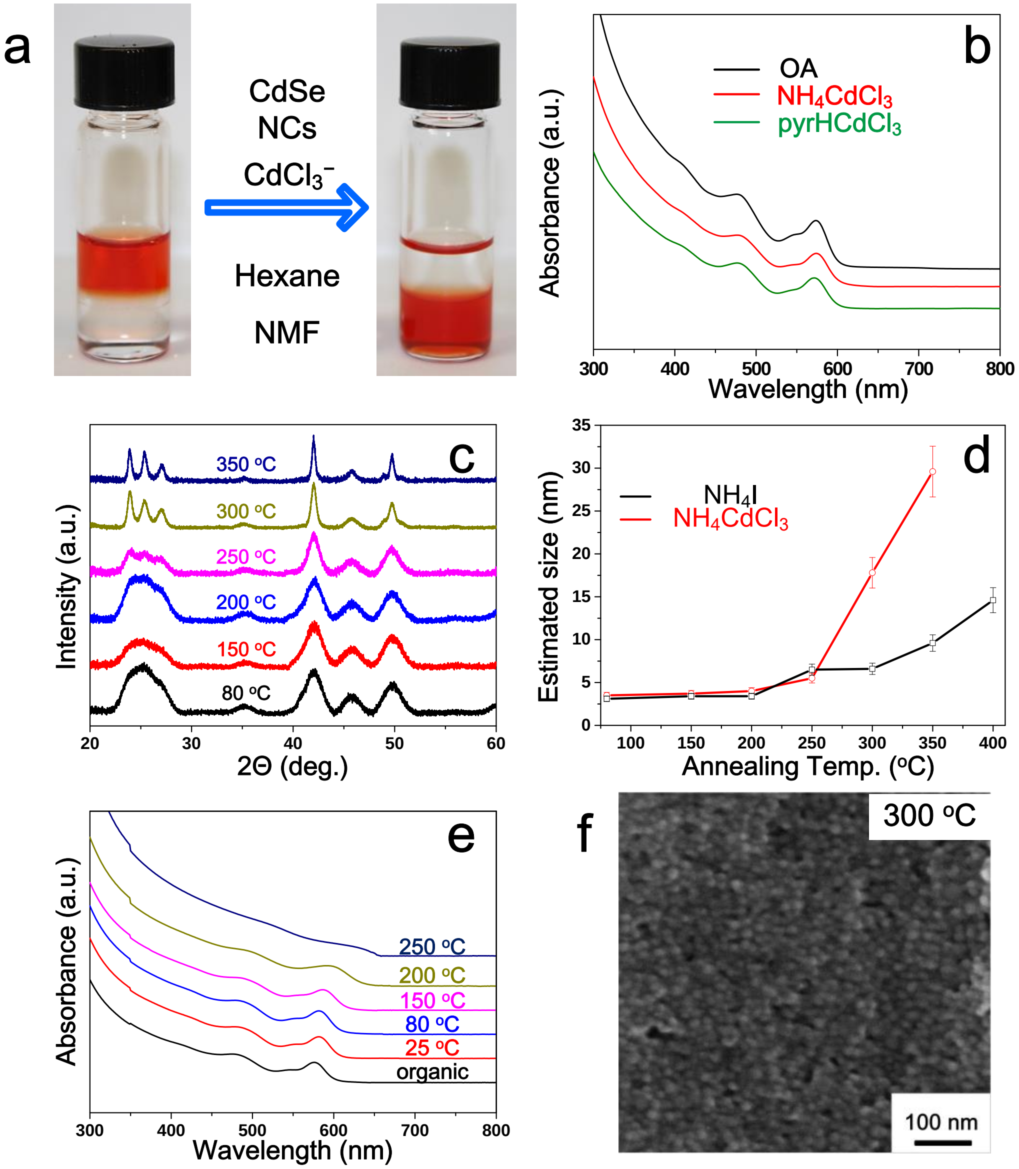

Figure 4.9. (a) A photograph showing the phase transfer of CdSe NCs from hexane to NMF in the presence of NH_4CdCl_3. (b) Comparison of UV-visible spectra of CdSe NCs capped with oleate (OA, in toluene) and $CdCl_3^-$ ligands (in NMF). (c) XRD patterns of $CdCl_3^-$-capped CdSe NCs after annealed at various temperatures. (d) Evolution of grain sizes (estimated by Scherrer's equation) of $CdCl_3^-$-capped CdSe NCs versus annealing temperatures. $CdCl_3^-$ catalyzes the grain growth compared to other inorganic ligands such as I^-. (e) Evolution of the absorption features of $CdCl_3^-$-capped CdSe NCs versus annealing temperatures. The spectrum for organically-capped CdSe NCs (black curve) is shown for comparison. (f) A SEM image of $CdCl_3^-$-capped CdSe NC thin film annealed at 300 °C, showing an average grain size of 15–20 nm, in accordance with the XRD results. For (c–e), to investigate the size evolution of the $CdCl_3^-$-capped CdSe NCs, the drop-cast thin films were annealed at various temperatures on a hot plate in a N_2-filled glove box.

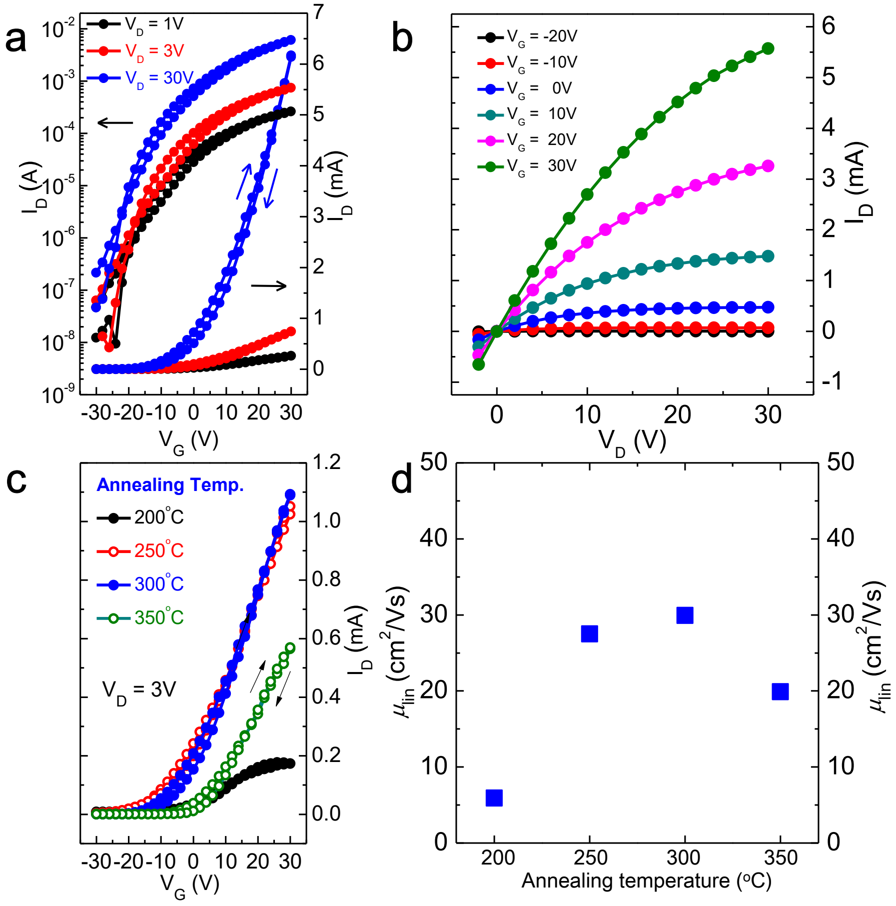

Figure 4.10. (a,b) Transfer and output characteristics for FETs of $CdCl_3^-$-capped CdSe NCs annealed at 300 °C (channel width, $W = 1500$ μm and channel length, $L = 125$ μm); (c) Transfer characteristics for $CdCl_3^-$-capped CdSe NC FETs annealed at various temperatures; (d) Dependence of μ_{lin} on annealing temperatures.

4.6.2. Overall outlook of halometalate ligand exchanges.

In conclusion, we have designed an ink of $CdCl_3^-$-capped CdTe NCs, which combines the photovoltaic active materials and the sintering promoters in a single solution. The dual role of $CdCl_3^-$ ligands allows a facile device fabrication with no need for $CdCl_2$ treatment. Solar cells made from this new ink show high PCE over 10%. Furthermore, we envisage the chemical design of NC-based materials through inorganic ligand chemistry can be generally applied to a broad scope of materials and fields. Materials of interest include $Hg_{1-x}Cd_xTe$ (MCT), $Cd_{1-x}Zn_xTe$ (CZT), and other II–VI alloys. MCT alloys are the prevalent materials for infrared photodetectors, while

CZT alloys are commonly used in high energy photon detection, especially X- and gamma-rays. The additional functionalities brought by surface ligands would contribute to better performance and improved manufacturing for NC-based devices in a wide variety of fields.

4.7. Acknowledgements.

This work was a collaborative effort that required many parts to come together. Dr. Hao Zhang was incredibly easy to work with as we developed this chemistry. It took time to figure out which solvent to choose, but it worked out. Jake Russell was extremely helpful when it came time to fully characterize the new material method. Prof. Jaeyoung Jang helped establish useful protocols for the CdSe transistors that helped to establish a baseline for CdTe. Prof. Dmitri Talapin helped guide the structure of the manuscript to make it worthy of JACS.

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5. Roll-to-roll friendly solution-processing of sintered cadmium telluride nanocrystal photovoltaics.

The following work was a collaboration with a number of people that is currently incomplete. However, it is closely linked with the other research and bears disclosure. It will go into rough detail of the process and refinement of many important factors for making CdTe nanocrystal solar cells industrially relevant.

5.1. Roll-to-roll friendly methods for depositing cadmium telluride nanocrystal inks.

Solution-processed solar cells made using roll-to-roll friendly techniques have garnered increasing interest over the past two decades as a low-cost alternative to single crystal silicon or chemical vapor deposited gallium arsenide thin films.[1] A wide variety of materials have been solution processed into photovoltaics, including organic polymers,[2-4] lead sulfide quantum dots (PbS QDs),[5-6] lead halide-based perovskites,[7-9] and sintered nanocrystals[10] (NCs) made from Cu(In,Ga)(S,Se)$_2$,[11-12] Cu$_2$ZnSn(S,Se)$_4$,[13-15] or CdTe.[16-17] Most of the top power conversion efficiencies (PCE) were achieved using spincoating to produce a uniform semiconductor layer. However, spincoating has many disadvantages: significant waste of material, mediocre scalability, low throughput, and limited substrate geometries. All of these factors limit cost reduction, speed of implementation, and flexibility desired from the transformation of new materials strategies into effective technologies. Promising substitutes include dip-coating,[18-19] doctor-blading,[20-21] and spraycoating.[22-23]

Many studies on sintered CdTe NC solar cells have been reported. Our method for roll-to-roll friendly CdTe solar cells utilizes recent advances to surface ligand chemistry,[24-26] understanding grain growth of NC solids,[27-28] and device interfaces.[29-30] Panthani et al. and MacDonald et al. improved the zinc oxide layer by changing from NCs to a sol-gel method as well as explored the poor contact between ITO and CdTe.[29-30] They found current/light soaking is a viable route to overcome the issue and probe the true limits of the deposited CdTe absorber layer. Both reports employ a saturated cadmium chloride ($CdCl_2$) bath to chemically treat the NC solid followed by heat treatment. By harnessing chlorocadmate ($CdCl_3^-$), first reported by Dirin et al. as NC surface ligands, Zhang et al. created an ink that can be solution-processed and annealed into a polycrystalline CdTe absorber layer without the need of additional chemical treatment.[24-25] They even showed the new ink can be integrated into roll-to-roll friendly techniques, such as spraycoating.

Spraycoating was proven effective at depositing PbS QDs,[31] perovskites,[23] and CdTe NCs.[32-33] Foos et al. spraycoated CdTe NCs onto indium tin oxide (ITO) coated glass and sintered the material into large grains of polycrystalline CdTe.[32] Calcium and aluminum were thermally evaporated to create a Schottky junction solar cell, resulting in PCE of 2.3%. Townsend et al. further improved the device efficiency by depositing zinc oxide (ZnO) sol-gel between the CdTe absorbing layer and top electrode, making a heterojunction solar cell that improved the device efficiency to 3.0%.[33] To date, there have been no reports on the deposition of CdTe NCs using doctor-blading as a method for making photovoltaic absorber layers. All reports on sintered CdTe NCs deposited by means of spraycoating have utilized $CdCl_2$ treatment, preventing ease of roll-to-roll fabrication.

We developed a method for combining roll-to-roll friendly techniques into a single, integrated process. Spraycoating and doctor-blading efficient CdTe solar cells was achieved by diluting a standard mixture of pyridine and 1-propanol (1-PA) with methanol. $CdCl_3^-$-capped CdTe

NCs were easily deposited with spraycoating or doctor-blading by adjusting the procedure outlined by Zhang et al. to improve solubility and increase film thickness for a single layer.[24] Infrared (IR) lamps were used to anneal the substrates during layer-by-layer deposition to replace the normal hot plate. All of these advances in CdTe absorber layer deposition seamlessly integrate into a single, roll-to-roll friendly process that can be adapted to different substrate geometries and materials.

5.2. Experimental route to developing an integrated roll-to-roll friendly process.

5.2.1. Chemicals used to develop a roll-to-roll friendly process.

Cadmium oxide (CdO, 99.99+%), tellurium shot (Te, 99.999%), cadmium chloride ($CdCl_2$, 99.99%), pyridinium hydrochloride (pyr·HCl, 98%), zinc acetate dihydrate ($Zn(OAc)_2 \cdot 2H_2O$, 99.999%), indium chloride ($InCl_3$, 99.999%), oleic acid (OA, technical grade, 90%), 1-octadecene (ODE, technical grade, 90%), tributylphosphine (TBP, 97% with isomers), toluene (≥99.8%, anhydrous), ethanol (≥99.5%, anhydrous), pyridine (99.8%, anhydrous), hexane (95%, anhydrous), *N*-methylformamide (NMF, 99%), hexamethylphosphoramide (HMPA, 99%), 1-propanol (1-PA, 99.7%, anhydrous), 2-methoxyethanol (99.9%, anhydrous), and ethanolamine (99.5%, redistilled) were purchased from Aldrich. Molecular sieves grade 564 (Type 3A, 8-12 mesh beads), acetone (certified ACS), methanol (certified ACS), and 2-propanol (IPA, certified ACS) were purchased from Fisher Scientific. Aluminum (Al, 99.99%) and silver (Ag, 99.99%) pellets were purchased from Kurt J. Lesker Company. PELCO colloidal silver paste (Ag paste) was purchased from Ted Pella, Inc. 10 wt% TBP:Te was prepared by dissolving 10 g of Te shot in 90 g of TBP overnight in a N_2-filled glove box. ODE was recrystallized by cooling the bottle in a chiller overnight at 12 °C and decanted to remove impurities. OA was cooled to 16 °C overnight and vacuum filtered to remove high melting point impurities. Pyridine, NMF, and 1-PA were distilled to remove low and high boiling point impurities. NMF and HMPA were dried over molecular sieves and filtered with 0.2 μm PTFE filter before use.

5.2.2. Cadmium telluride nanocrystal ink preparation.

5.2.2a. Oleate-capped cadmium telluride nanocrystal synthesis.

CdTe NCs capped with oleate were synthesized with a modified method described by MacDonald et al.[17,30] In short, 4.80 g CdO, 42.4 g recrystallized OA, and 40.0 g recrystallized ODE were charged in a 500 mL flask and evacuated overnight to remove trace oxygen. The flask was heated to 80° C until the pressure equilibrated. Under dry nitrogen, the mixture was heated to 220° C until the solution turned clear, indicating a completed reaction. The flask was cooled to < 90° C and evacuated. The flask was heated to 110° once the solution stopped bubbling and left until the pressure equilibrated. Under dry nitrogen, the flask was heated to 270° C and 24 mL of 10 wt% TBP:Te were injected. The heating mantle was removed immediately and the flask was allowed to air cool to <50° C. The resulting CdTe NC solution was split evenly and purified using anhydrous toluene and ethanol as the solvent/non-solvent combination.

5.2.2b. Pyridine-capped cadmium telluride nanocrystal ink.

Following 4-6 purification cycles, CdTe NCs were redispersed in anhydrous pyridine at a concentration of ~80 mg/mL. The solution was stirred under N_2 overnight on a hotplate set to 100 °C, followed by precipitation using hexane. The CdTe NC precipitates were redispersed in fresh pyridine to prepare the pyridine-capped CdTe NC stock solution. The stock pyridine-capped CdTe NC solution was precipitated by hexane and dissolved in a 1:1 mixture of pyridine and

1-PA to the desired concentration. The solution was sonicated for 10 min and filtered through a 0.2 μm PTFE syringe filter to prepare the spincoating solution.

5.2.2c. Trichlorocadmate-capped cadmium telluride nanocrystal ink.

The procedure was adapted from a process established previously by Zhang et al.[24] In short, chlorocadmates ($CdCl_3^-$) with pyridinium (pyr-H^+) cations were synthesized by mixing equimolar amount of $CdCl_2$ and pyr·HCl in NMF (0.1 M). In a typical ligand exchange, 18 mL of oleate-capped CdTe NC (Section 2a) solution in hexane (~30 mg/mL) was mixed with 18 mL of $CdCl_3^-$ solution in NMF (0.1 M). Under vigorous stirring, NCs gradually transferred from hexane to NMF. Upon phase transfer, the bottom phase containing CdTe NCs was then rinsed with fresh hexane three times.

Following the $CdCl_3^-$ ligand exchange, a mixture of toluene (6 mL) and HMPA (3 mL) was added, leading to the flocculation of NCs in solution. The NC precipitates were collected by centrifugation, and re-dispersed in 5 mL of pyridine. The solution of $CdCl_3^-$-capped CdTe NCs in pyridine was vigorously stirred for ~2 hrs in air, followed by centrifugation to remove the insoluble part. An equal amount of 1-PA was added to the NC solution in pyridine to make the “original” ink.

5.2.2d. “Overwashed” trichlorocadmate-capped cadmium telluride nanocrystal ink.

Following $CdCl_3^-$ ligand exchange (Section 5.2.2c), the NCs were precipitated with the same non-solvent mixture outlined previously. However, instead of re-dispersing in pyridine, the NCs were dissolved in NMF (~18 mL). The same precipitation and re-dispersing procedure was repeated. Following a third precipitation, the NCs were re-dispersed in 2.5 mL pyridine and stirred vigorously for ~2 hrs. The solution was centrifuged to remove insoluble NCs and a concentration was calculated to be described later. Additional pyr·$HCdCl_3$ ligand solution in pyridine was added to the NC solution in varying amounts to replenish Cl necessary for grain growth. An equal amount of 1-PA was added to the solution to make the "overwashed" ink.

5.2.3. Cadmium telluride absorber layer deposition.

5.2.3a. Substrate preparation.

In detail, 25 mm×25 mm indium tin oxide (ITO)-coated glass substrates (Thin Film Devices Inc.) were cleaned by sequential sonication in deionized water (DI) and Alconox detergent, DI, acetone, IPA, and DI. Afterward, the substrates were dried under N_2, and hydrophilized for 10 min using a Harrick PDC-001 Extended Plasma Cleaner.

5.2.3b. Spincoating of cadmium telluride nanocrystal ink.

The CdTe NC inks outlined previously (Section 2b, c.i, & c.ii) was spincoated using the following procedure. Onto freshly plasma treated (Section 3a) ITO substrates, the CdTe NC ink was pipetted (~250 μL) onto the substrate and spun at 800 rpm for 30 s followed by 2000 rpm for 10 s. The substrate was transferred to a hot plate and dried at 150 °C for 2 min.

5.2.3c. Spraycoating of cadmium telluride nanocrystal ink.

The CdTe NC ink outlined previously (Section 2b, c.i, & c.ii) was diluted with methanol by 6 parts methanol to 1 part NC solution. The layer thickness was controlled by changing the NC concentration in 1:1 pyridine:1-PA. A homemade spraycoating system was built by using a hot plate and a Paasche airbrush set to 45° to create a thinner wetting layer. The ink was loaded into the airbrush and sprayed briefly to wet the surface. The spray was controlled by solenoid valves attached to a power supply. The substrate was heated to 38 °C to facilitate drying. The spraycoating system was upgraded by making a metal turntable heated to 38 °C to move the substrates through the spray and process multiple substrates at a time. The spray nozzle was upgraded to VMAU-316SS spraying assembly from Spraying Systems Co. to more easily adjust spray parameters. Upon deposition, the substrate was dried at 150 °C for 2 min.

5.2.3d. Doctor-blading of cadmium telluride nanocrystal ink.

The same ink preparation procedure outlined for spraycoating (Section 3b.ii) was used. An Al block was heated on a hot plate to 40 °C to facilitate smooth deposition. Glass slides were placed onto the block to act as height guides. A small amount of the NC solution (~75 μL) was pipetted onto the substrate and a glass rod was used to smooth the film by moving back and forth. The excess was wicked away by sweeping the rod onto the glass slides. Upon deposition, the substrate was dried at 150 °C for 2 min.

5.2.4. Chemical and thermal treatment of cadmium telluride absorber layers.

5.2.4a. Cadmium chloride bath and annealing for pyridine-capped cadmium telluride nanocrystal ink.

For the $CdCl_2$ treatment, the substrate was cooled in air and was dipped into a saturated $CdCl_2$ bath in methanol at ~60 °C for 15 s, thoroughly rinsed with IPA and dried under N_2 flow. The substrate was annealed at 350 °C on a hot plate (or under an IR lamp shielded with Al foil) for 20 s and cooled in air. The whole process (deposition, drying, $CdCl_2$ treatment, thermal treatment) was repeated multiple times (12–20) until the desired thickness was achieved.

5.2.4b. Annealing for trichlorocadmate-capped cadmium telluride nanocrystal ink.

For $CdCl_3^-$-capped CdTe NC inks, there was no need for a $CdCl_2$ bath treatment. Instead, the substrate was transferred directly from the drying plate to the annealing plate. The substrate was annealed at 350 °C on a hot plate (or under an IR lamp shielded with Al foil) for 20 s and cooled in air. The whole process (deposition, drying, annealing) was repeated multiple times (12–20) until the desired thickness was achieved.

5.2.5. Spraycoating onto curved substrates.

Glass rods, beads, and plano-convex lenses were purchased from various outside vendors. They were affixed to the spraycoater using double sided tape. For full devices, special holders would be necessary to assure consistency as well as reduce mistakes from processing difficulties.

5.2.6. Finishing sintered cadmium telluride nanocrystal solar cells.

5.2.6a. Indium-doped zinc oxide sol-gel n-type layer.

The ZnO layer was deposited on top of CdTe by spin-coating 300 μL of ZnO sol-gel at 3000 rpm for 30 s, followed by annealing at 300 °C for 2 min. The ZnO sol-gel was prepared by sonicating a mixture of 1.50 g of $Zn(OAc)_2{\cdot}2H_2O$, 15 mL of 2-methoxyethanol, 420 μL of ethanolamine, and 15–45 mg of $InCl_3$ for 1 h, and subsequently stirred overnight.

5.2.6b. Aluminum/silver electrode deposition.

The substrates were transferred into a glove box and kept under high vacuum (~10^{-9} Torr) overnight. Top Al contacts (100 nm) were deposited by thermal evaporation through a homemade mask, featured by evenly distributed 8 mm^2 holes. Ag (100 nm) was deposited on top of Al to increase device longevity. Three sides of the device stack were scratched off to expose the ITO. Electrical contact was established using Ag paint.

5.2.7. Materials characterization techniques.

The optical absorption spectra of NC solutions were collected using a Cary 5000 UV-Vis-NIR spectrophotometer in the transmission mode. Scanning electron microscopy (SEM) images of the complete CdTe solar cell devices were acquired on Zeiss-Merlin. X-ray photoelectron spectroscopy (XPS) analysis was performed on a Kratos AXIS Nova spectrometer using a monochromatic Al K_α source (hν = 1486.6 eV). The Al anode was powered at 10 kV and 15 mA. Instrument base pressure was 1×10^{-9} Torr. High-resolution spectra in Cd 3d, Te 3d, C 1s, Cl 2p and P 2p regions were collected using an analysis area of 0.3×0.7 mm^2 and 20 eV pass energy.

5.2.8. Photovoltaic characterization.

Devices were tested under the illumination of a Xe lamp with a AM 1.5G filter (Newport 67005) and calibrated with a Si photodiode with a KG5 filter (Hamamatsu Inc, S1787-04). The illumination area was controlled by a self-aligning stainless steel aperture mask with evenly distributed, nominally 6 mm^2 circular holes (5.94 mm^2 measured). Current density versus voltage (JV) curves were acquired using a Keithley 2400 sourcemeter controlled by a Labview interface. To mitigate heating during measurements, the perimeter of the cell was in direct contact to an Al heat sink. The instruments were controlled and data collected using a homemade Labview program. Current/light soaking was done by applying 2–3 V (forward bias) to the device under illumination for varying amounts of time. Typically, this generated a current density of ~2.5 A cm^{-2}. The current was monitored carefully to not exceed a 3 A cm^{-2}, as current densities greater than this generally caused performance degradation. Holding the devices in reverse bias generally caused a transient decrease in performance (due to reduced V_{OC}). External quantum efficiency (EQE) measurements were taken using Oriel IQE-200 with a step of 20 nm for the wavelength. Capacitance-voltage (Mott-Schottky) data were acquired using a Gamry Reference 600 potentiostat. Data were acquired using a frequency of 500 Hz with an amplitude and step size of 5 and 10 mV, respectively.

5.3. Transitioning from spincoating to spraycoating or doctor-blading.

We created a procedure that combines doctor-blading (or spraycoating), $CdCl_3^-$ chemistry, and IR lamps integrated into a roll-to-roll friendly process (Figure 5.1). Transitioning to spraycoating or doctor-blading allows for a continuous process stream without the need to load the substrate onto a platform that grips it. $CdCl_3^-$ chemistry eliminates the need for the $CdCl_2$ treatment, a tedious and difficult to reproduce process. Instead, the ink is self-contained, comprising the CdTe NCs and the $CdCl_2$ grain growth promoter. Changing from a hot plate to an IR lamp proves the substrate does not need to be heated from the glass side to create continuous grains of CdTe throughout the film. IR lamps allow the substrate to simply move through a heated zone instead of requiring a hot surface.

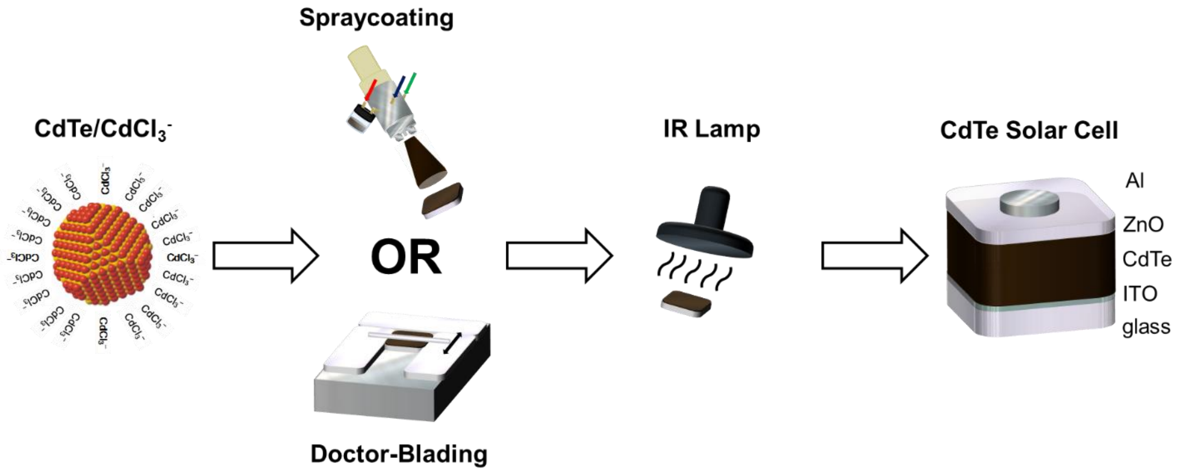

Figure 5.1. Schematic combining roll-to-roll friendly techniques into a single process.

Spincoating is not conducive to roll-to-roll fabrication because it scales poorly to large areas, wastes considerable amounts of material, is not a high throughput deposition method, and limits the geometry to planar substrates. All of these factors make other deposition methods, such as spraycoating or doctor-blading, better alternatives. Spincoating is a materials inefficient method for depositing any ink. 200 μL of 40 mg/mL NC ink was required to cover a single 25 mm x 25 mm substrate. Over the course of 20 layers, ~500 nm of CdTe is deposited onto the substrate. This means about 160 mg of NC is required to deposit ~1.9 mg of CdTe, conservatively. The result is only ~1% of material remains on the substrate during spincoating. For the same thickness device, 80 mg of CdTe NC is required during spraycoating and only 2 mg is required for doctor-blading. Unlike spincoating, spraycoating can accommodate larger substrates without significant change to the film consistency. Larger areas also become more materials efficient. These techniques were both attempted without the benefit of process engineers optimizing it. Literature reports spraycoating efficiencies as high as ~95% by Gilmore et al.[34] We made devices with roughly the same efficiencies using spraycoating and doctor-blading (Figure 5.2).

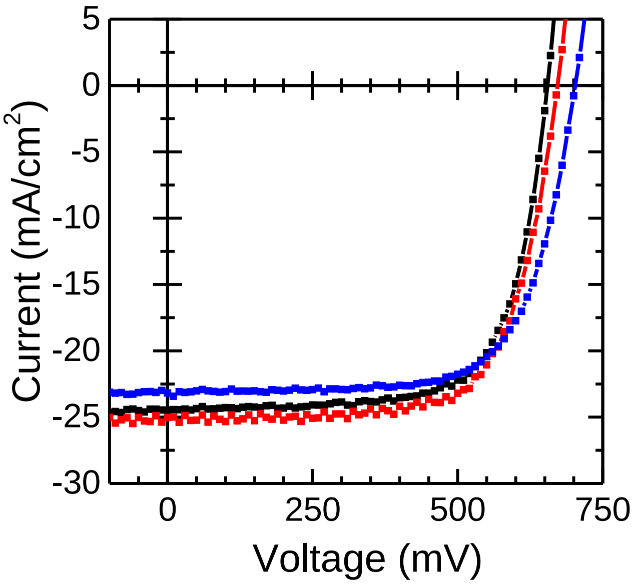

Figure 5.2. JV curves under AM1.5G illumination for spincoated (black), spraycoated (red), and doctor-bladed (blue) CdTe absorber layers.

The devices made using roll-to-roll friendly techniques were comparable to spincoated devices. Both techniques proved effective at consistently improving V_{oc}, a device parameter that typically depends more on device architecture than processing conditions. This is a good indication that the CdTe absorber layer is denser with fewer defects that contribute to Shockley-Read-Hall recombination and increase shunting. J_{sc} showed as much variability as is typical for the CdTe NC ink. JV curves in the dark helps to illustrate relative film quality (Figure 5.3).

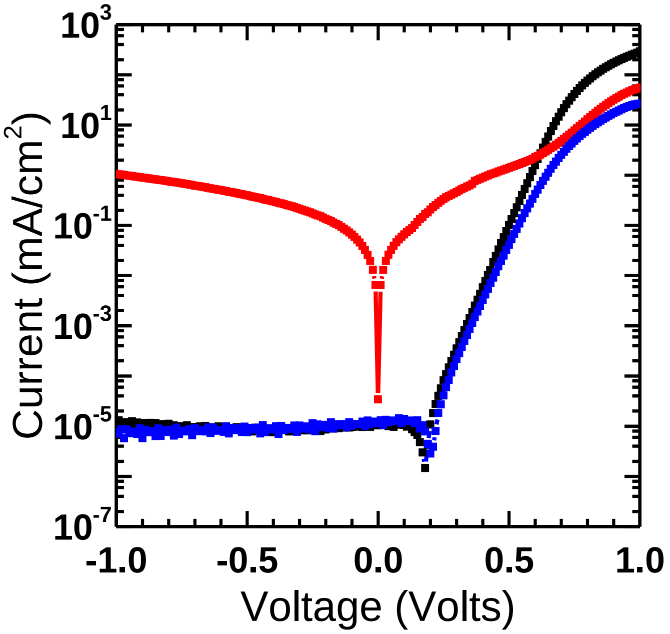

Figure 5.3. JV curves in the dark of spincoated (black), spraycoated (red), and doctor-bladed (blue) CdTe absorber layers made into completed devices.

5.4. Experiments to finish the work.

There are a few experiments I need to do to finish off this work. I need to make devices using the overwash procedure to properly compare the new conditions. This will help to compare how different controls affect the overall device properties. I will also need to fully characterize how the IR lamp affects the sintering process. This will entail performing top-view SEM and XRD. Finally, I will combine with improved deposition methods, overwash procedure, and IR lamp to fully integrate the process. This will prove that they can be combined without detriment to device performance.

5.5. Acknowledgements.

The above work was a collaboration of many people. Dr. Hao Zhang provided a large amount of insight for the subtle changes to the ligand exchange and the subsequent materials characterization. Jia-Ahn Pan contributed greatly to developing the overwash procedure and laid

the foundation for the improved nanocrystal ink. Jake Russell helped to design and improve the new deposition methods, laying the groundwork of the entire project. Dr. Gregory Pach and Bobby To helped to image the cross-sections of the device stack. Prof. Dmitri Talapin guided the entire work and provided valuable insight into assembling the work into a coherent project.

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6. Conclusions.

6.1. Overview of the contributions to solution-processed cadmium telluride photovoltaics.

Over the course of my graduate school career, we developed a platform for testing CdTe deposition, created Ohmic contacts to sintered CdTe with solution-processed materials, designed a new nanocrystal ink, and assembled a roll-to-roll friendly process. All of these contributions improved understanding necessary for making solution-processed solar cells a reality. To controllably test new chemistries, it is important to have an effective method to isolate variables to properly monitor effects from the changes made. We designed to understand how this device architecture optimally works to create a baseline solar cell to which all future research can be compared. From there, we created new methods for developing transparent Ohmic contact to solution-processed CdTe. By adding a different material at the ITO/CdTe interface, we were able to achieve efficiencies of ~7% that were stable over 1 week, and even longer. We also successfully combined CdTe nanocrystals with $CdCl_3^-$ ligands to create an ink that contained the semiconductor with the requisite grain growth agent. The new ink proved effective at creating photovoltaic-grade CdTe without an additional $CdCl_2$ bath step. Finally, through improved deposition techniques, we developed a roll-to-roll friendly process for fabricating CdTe solar cells. We were able to deposit with spraycoating or doctor-blading the new nanocrystal ink, altered for better stability and control. The deposited material can be annealed with an IR lamp without negatively affecting device performance. All of these changes can seamlessly integrate with one another, making it possible to assimilate this technology into a high throughput fabrication process.

6.2. Outlook of nanocrystal research for solution-processed electronics.

I think nanocrystals have a large amount of value to offer semiconductor research in the future. Now that we have developed new methods for solubilizing and depositing nanocrystals, we can start working with more complex systems. For sintered CdTe nanocrystal solar cells to become a viable technology, we need to better understand grain boundaries. Nanocrystal chemistry offers an effective method for controllably understanding how semiconductor grains grow and the role grain boundaries play. Nanocrystals applied towards solar energy will have difficulty gaining traction in real world applications since CdTe is already the cheapest solar material (close between CdTe and polycrystalline Si). The nice thing about this research is it can easily be applied to other materials systems. One avenue I think worth pursuing is alloying different II-VI semiconductors together to control the band gap. It is a very common method in the materials science world, but little work has been done in this area for sintered nanomaterials. It becomes especially important when trying to implement new device design, because this is an effective method for adjusting the energy levels without having to maintain quantum confinement. Mercury cadmium telluride has yet to be solution-processed, and it is arguably one of the most relevant semiconductors in real world applications.

In my work with Dr. Wenyong Liu, he showed me some interesting trends in nanocrystal sintering that I think would be worth exploring as well. III-V nanocrystals tend not to sinter upon heating, making them ideally suited for sustained quantum confinement. From this interesting observation, I think it would be worth pursuing III-V/II-VI hybrid materials for use in LEDs. By lattice matching II-VI materials to III-V nanocrystals, size controlled nanocrystals can be controllably suspended in a conductive matrix. Polycrystalline materials have better stability, making this an appealing approach to long term applications. I have already talked with Dmitri about many of these possibilities and what would be useful approaches to such problems.